Single Active Block-Based Emulators for Electronically Controllable Floating Meminductors and Memcapacitors

Mihajlo TATOVIC, Predrag B. PETROVIC

Dept. of Electronics, Faculty of Technical Sciences Čačak, University of Kragujevac, Svetog Save 65, 32000 Čačak, Serbia

mihajlo.tatovic@ftn.kg.ac.rs, predrag.petrovic@ftn.kg.ac.rs

Submitted September 4, 2023 / Accepted October 23, 2023 / Online first November 6, 2023

Abstract. *This paper introduces two novel emulator circuits that employ a single active block. The first circuit utilizes a Voltage Differencing Transconductance Amplifier (VDTA) to emulate the behavior of a floating/grounded incremental/decremental flux-controlled meminductor. The second circuit, based on a Voltage Differencing Current Conveyor (VDCC), emulates the characteristics of memcapacitance. Both emulation circuits are constructed using capacitors as the only type of grounded passive element. Notably, these circuits possess electronic tunability, enabling control over the realized inverse meminductance/memcapacitance. The theoretical analysis of the proposed emulators includes an investigation into potential non-idealities and parasitic effects. By carefully selecting the passive circuit elements, efforts were made to minimize the impact of these unwanted effects. In comparison to existing designs documented in the literature, the proposed circuits demonstrate remarkable simplicity. Additionally, they exhibit wide frequency operability (up to 50 MHz) and successfully pass the non-volatility test. Simulation results conducted using 0.18 μm CMOS technology and a ±0.9 V supply voltage align closely with the theoretical predictions. Furthermore, Monte Carlo simulations and corner analysis are employed to evaluate the circuit's robustness. To validate the feasibility of the proposed solution, experimental tests are performed using commercially available components.*

Keywords

Meminductor, memcapacitor, emulator, VDTA, VDCC, grounded passive components, electronic controller, simulation

1. Introduction

The increasing demand for intelligent technological solutions has prompted researchers to establish more intricate requirements in both research and the development of complex systems. These systems necessitate the harmonious operation of subsystems with varying physical characteristics. In order to model nonlinear phenomena occurring in diverse physical processes, resistors, capacitors, and inductors are commonly employed as fundamental building elements. These elements embody the essential relationships between current, electrostatic, and magnetic fields, serving as a means to describe reality and adhere to the fundamental laws governing it. In 1971, the concept of the memristor was introduced [1], expanding the trinity of basic elements. Subsequently, in 1980, other members known as Higher Order Elements (HOEs) were introduced [2–4]. The memristor concept was further extended to encompass meminductors and memcapacitors. These components belong to a class of two-terminal devices, wherein their inductance or capacitance is determined by the internal state of the system. Although these components are still in the experimental and theoretical stages, researchers are exploring various potential applications for them in real-life scenarios [5]. Meminductors and memcapacitors could be used in energy storage systems, such as inductors and capacitors in power supplies. Their ability to "remember" past magnetic flux and charge levels could lead to the development of more efficient and responsive energy storage devices - by utilizing the memory effect, these components can optimize the use of energy in electronic circuits, leading to energy savings in various applications. Meminductors can be utilized in analog signal processing circuits. They could enable the creation of adaptive filters and oscillators, which can adjust their parameters based on past signals, leading to more efficient and adaptive signal processing systems. In RF circuits, meminductors and memcapacitor could be employed to create tunable inductors and capacitors which could be used in wireless communication devices, enabling the tuning of frequencies and improving the efficiency of RF circuits. Meminductors, similar to memristors, could be applied in neuromorphic computing to simulate synaptic behavior - to mimic the plasticity of biological synapses in artificial neural networks. Memcapacitors can store and release electrical energy in response to changing capacitance values. This property makes them suitable for energy harvesting applications where variable energy sources, such as solar or vibration energy, need to be efficiently captured and stored. Memcapacitors can store analog information, making them potentially useful in analog memory devices, analog computing and signal processing, where the ability to retain analog information is crucial. Also, they can be integrated into sensors to detect various physical parameters such as pres-

DOI: 10.13164/re.2023.0568

sure, humidity, or displacement - their ability to store charge based on these parameters can lead to the development of responsive and adaptable sensor systems.

The research on memelements, particularly meminductors and memcapacitors, has gained significant attention in the past two decades, primarily due to their lack of physical solid structure. To effectively develop these elements, emulator circuits must replicate the key characteristics of ideal memelements, which are well-defined by theoretical principles [1–5]. Moreover, these emulator circuits need to be compatible with CMOS technology to ensure practical implementation and validation. In light of the aforementioned requirements, the emulator circuits should exhibit control over both AC and DC performance parameters, encompassing a wide operating frequency range. Current mode (CM) active blocks are often favored as the foundation for designing new emulator solutions. This preference stems from their advantages, such as low power consumption, extensive frequency coverage, and minimal parasitic effects. In comparison, standard operational amplifiers (OAs) demand higher DC power and exhibit lower operating frequencies with increased parasitic impacts compared to CM circuits. Additionally, incorporating a multiplier in the circuit adds complexity and reduces the achievable operating frequency.

Given the current expectation that the commercial availability of meminductors and memcapacitors is unlikely in the near future, researchers have developed various types of SPICE models [6–8] and emulator circuits [9–35] to investigate the dynamics of such devices. To simulate the behavior of meminductive/memcapacitive devices, researchers have employed mutator circuits that can convert memristors into either meminductive or memcapacitive elements [9], [10]. For instance, a voltage differencing current conveyor (VDCC)-based mutator circuit capable of operating up to 700 kHz was introduced in [10], while a universal emulator based on commercial OTA and CCII circuits was proposed in [11]. Another approach by Vista and Ranjan [12] utilized two voltage difference transconductance amplifiers (VDTAs) and one multiplier in their meminductive emulator (MIE), which achieved operation up to 1 MHz. In [13], an operational transconductance amplifier (OTA)-based MIE was presented; however, its operational frequency was limited to 10 kHz, and a multiplier was required. Raj et al. [14] proposed an MIE employing three OTAs, which operated up to 10 MHz, but the capacitor value at 10 MHz was only 1 pF. Kumar and Nagar [15] introduced an MIE employing a VDTA and OTA, with an operational frequency of up to 3 MHz, but the capacitor value of 2 pF was deemed impractical. Bhardwaj and Srivastava [16] suggested an MIE employing two VDTAs, which operated up to 1.5 MHz. Orman et al. [17] devised an MIE employing a differential difference current conveyor (DDCC) with both hard and smooth switching behaviors. Yadav et al. proposed an MIE utilizing two OTAs and one current differencing buffered amplifier (CDBA), operating up to 2 MHz; however, this implementation necessitated 37 CMOS transistors and six current sources, which was considered excessive [18]. Bhardwaj and Srivastava devised an MIE employing a modified VDCC (MVDCC) and OTA, requiring a total of 38 transistors and operating up to 300 kHz. Additionally, it necessitated one resistor and two capacitors [19]. Petrovic [20] expanded the concept of the voltage difference transconductance amplifier (VDTA) to a multiple-output VDTA (MO-VDTA) and proposed an MIE employing a single MO-VDTA, while a compact emulator structure which realizes the behavior of a floating meminductor and memristor employing a single VDIBA (a voltage differencing inverted buffered amplifier) and a dual-output OTA was proposed in [21].

Regarding memcapacitor emulators, these emulators can be classified into two groups: grounded [11, 27–29, 31, 32, 34, 35] and floating [9, 10, 24–26, 30, 33]. Grounded memcapacitors require fewer active and passive components compared to floating memcapacitors, but their application range is more limited. Conversely, designing floating memcapacitors is more challenging than grounded ones. In the case of floating memcapacitors, their electronic tunability is a notable feature, although their performance is primarily evaluated through simulation results. For instance, Vista and Ranjan [24] proposed a floating memcapacitor based on a dual X current conveyor differential input transconductance amplifier (DXCCDITA), which utilized a single DXCCDITA and three passive elements. Other floating memcapacitor circuits [9, 10, 24] also possess electronically tunable characteristics, albeit their performance verification is limited to simulation results. In [25], a floating memcapacitor employing a varactor diode is presented, comprising four AD844s, one TL084, six resistors, two capacitors, and a single varactor diode. Sharma et al. [26] proposed a floating charge-controlled memcapacitor that incorporates two CCIIs, one multiplier, and three passive elements. The performance of this floating memcapacitor circuit is evaluated through both simulation and experimental results; however, it lacks electronic tunability. Ananda et al. proposed a floating memcapacitor consisting of two OTAs, one unity gain amplifier (UGA), and two MOS capacitors in [30]. In their more recent work in 2023 [33], Ananda et al. introduced a floating memcapacitor circuit employing one voltage difference transconductance amplifier (VDTA), one OTA, one buffer, and four passive elements. The maximum operating frequencies of these circuits [30], [33] are 1.2 MHz and 24 MHz, respectively. It is worth mentioning that the number of active and passive elements in the aforementioned floating memcapacitors exceeds those utilized in the memcapacitor proposed in this paper. A charge-controlled memcapacitor emulator using a VDCC and an OTA with grounded passive elements was described in [34].

This study proposes the design and implementation of floating meminductor and memcapacitor emulators utilizing a single active block, enabling electronic control over their characteristics. Moreover, this innovative design improves practical performance by mitigating the impact of existing nonlinearities. The proposed MIE circuits are

based on the Voltage Differencing Transconductance Amplifier (VDTA) and utilize the well-established and validated configuration of the Arbel-Goldminz Operational Transconductance Amplifier (OTA) cell [36]. These circuits offer several advantages over alternative active elements. Firstly, they require a reduced number of transistors in their implementations, leading to improved efficiency. Secondly, they provide enhanced controllability, allowing for precise manipulation of circuit parameters. Additionally, the ports of these circuits exhibit favorable impedance characteristics, further contributing to their performance. One notable advantage of the proposed MIE circuits is the elimination of special bias sources, which effectively removes body effects across all transistors. This simplifies the circuit design and ensures consistent behavior. The circuits feature a simple and symmetrical structure, accompanied by excellent impedance levels at the input and output. As a result, they can be easily connected in cascade or with other circuits without the need for specialized buffering. Moreover, the implementation of component matching is unnecessary in these circuits. The adopted OTA design guarantees minimal imperfections in terms of voltage and current gain, thereby achieving high accuracy in signal processing. Furthermore, the proposed structure exhibits low power dissipation and is capable of effectively driving a grounded load with a bipolar signal. In this study, a floating flux-controlled MIE is proposed, which utilizes only one VDTA, a V-I converter, and two grounded capacitors. This configuration is preferred over a grounded meminductor emulator as it is more suitable for circuit applications. To ensure operation in the high-frequency range, a MOS-capacitor is employed instead of a standard capacitor. The flux value of the emulator circuit can be adjusted by manipulating the transconductance gain through the biasing voltage of the VDTA. Unlike many previously known solutions, this approach does not rely on mutators, memristors, or multiplier circuits to achieve the desired current-flux characteristic. The avoidance of multiple multipliers in the design eliminates unnecessary bulkiness, making the proposed circuits more compact and efficient.

On the contrary, the proposed Charge-Controlled Memcapacitive Emulator (MCE) is based on utilizing the Voltage Differencing Current Conveyor (VDCC), which combines an Operational Transconductance Amplifier (OTA) with a modified current conveyor. This approach leverages the benefits of the second generation current conveyor (CCII), including a wide dynamic range, improved linearity, and a large signal bandwidth. Furthermore, it minimizes the number of floating elements typically found in CCII applications. [37] demonstrated a single VDCC-based configuration of the charge-controlled memristor based on grounded passive elements, while [35] used VDCC as a basic active element for realization of MCE but with much complex configuration then proposed in this study. The VDCC enables the realization of circuits in both differential and dual input modes. It offers electronically tunable transconductance gain and allows for the transfer of voltage through its relevant terminal. A key advantage of the proposed design is that it eliminates the need for component or parameter matching conditions. In the proposed floating memcapacitance mode, the circuit provides the flexibility to choose between soft or hard switching mechanisms (as memristor described in [38]) by adjusting the value of the capacitance or the frequency of the current excitation signal - switches from high capacitive state to low capacitive state suddenly. Altering the operating frequency and amplitude of the input current signal affects the width of the pinched hysteresis loop. Emulators with hard switching behavior, like the one proposed, find application in spiking and bursting neuron circuits as they exhibit two states: high and low memcapacitance.

The functionality of the presented emulators has been validated through Cadence Virtuoso simulations conducted using 0.18 μm CMOS technology. The experimental results, based on commercially available off-the-shelf components, demonstrate good agreement with the theoretical and simulation results. The proposed floating MIE and MCE emulators possesses the following benefits: it employs only one active elements; the necessary passive elements (two capacitors and electronically realized resistor) are grounded - the proposed MIE is resistor-less; it requires no external voltage multiplication circuitry (usage of one or more multipliers makes these configurations bulky in size); it provides electronic controllability features (by a bias voltage); it does not need any type of component/parameter matching condition; it offers the maximum operating frequency of up to 50 MHz – confirmed through simulation; low power consumption; it does not require mutation through external memristor to realize memcapacitor/meminductor elements. In the proposed MCE, the circuit offers the possibility of choosing the switching mechanism - soft or hard, by modifying the value of the capacitance used, or the frequency of the current excitation signal. Overall, the proposed emulators offer a simple, compact, and versatile design that is area efficient - utilization of grounded capacitors suitable for monolithic IC fabrication, and a reduced number of transistors.

By leveraging advanced circuitry techniques, these emulators offer a novel approach to simulate the behavior of floating meminductors and memcapacitors, crucial components in emerging electronic systems. The proposed design demonstrates promising results in terms of accuracy and controllability, opening up new avenues for research and practical applications in diverse fields such as memristor-based neural networks, adaptive filters, and energy storage systems.

2. Proposed Configurations

Figure 1 illustrates the proposed configurations of the emulator circuits for floating meminductor and memcapacitor.

The MIE depicted in Fig. 1(a) employs two MOSFETs, two capacitors, and one VDTA [20], [39]. The initial stage of the MIE comprises a VDTA, while the subsequent stage involves a MOSFET-based voltage-to-cur-

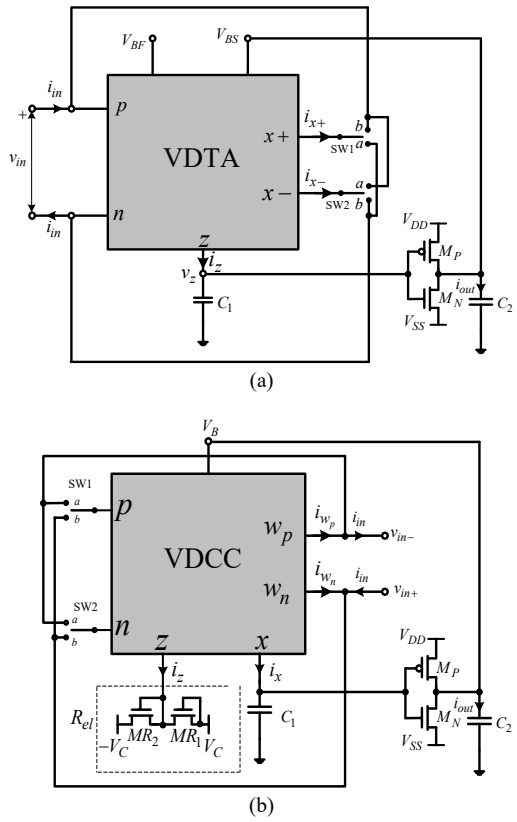


Fig. 1. (a) Floating meminductor emulator circuits based on VDTA. (b) Floating memcapacitor emulator based on VDCC.

rent (V-to-I) converter. Equation (1) provides the current-voltage relationships between the different ports of the Voltage Differencing Transconductance Amplifier (VDTA).

$$\begin{bmatrix} i_{\mathrm{z}} \\ i_{\mathrm{x+}} \\ i_{\mathrm{x-}} \end{bmatrix} = \begin{bmatrix} \beta_{\mathrm{F}} g_{\mathrm{mF}} & -\beta_{\mathrm{F}} g_{\mathrm{mF}} & 0 \\ 0 & 0 & \beta_{\mathrm{S}} g_{\mathrm{mS}} \\ 0 & 0 & -\beta_{\mathrm{S}} g_{\mathrm{mS}} \end{bmatrix} \begin{bmatrix} v_{\mathrm{p}} \\ v_{\mathrm{n}} \\ v_{\mathrm{z}} \end{bmatrix}. \quad (1)$$

The transconductance gains of the Voltage Differencing Transconductance Amplifier (VDTA), denoted as g_{mF} and g_{mS}, are electronically controlled by biasing voltage or current. The tracking errors of the first and second stages of the VDTA, represented as β_{F} and β_{S} respectively, define these gains. These parameters can be perceived as non-ideal transconductance gains of the VDTA stages, with typical values falling within the range of 0.9 to 1. An ideal value for these gains is 1. The VDTA can be characterized as a cascade of two stages: a differential-input-single-output (DISO)-type operational transconductance amplifier (OTA) followed by a single-input-dual (complementary)-output (SIDO)-type OTA. This characterization, along with the CMOS realization depicted in Fig. 2(a), clarifies the equivalent structure of the VDTA [20], [39].

The CMOS implementation of the Voltage Differencing Transconductance Amplifier (VDTA) is presented in Fig. 2(a). This realization involves the integration of two Arbel-Goldminz (AG) transconductance cells [33]. In this configuration, the transconductance gains g_{mF} and g_{mS} are

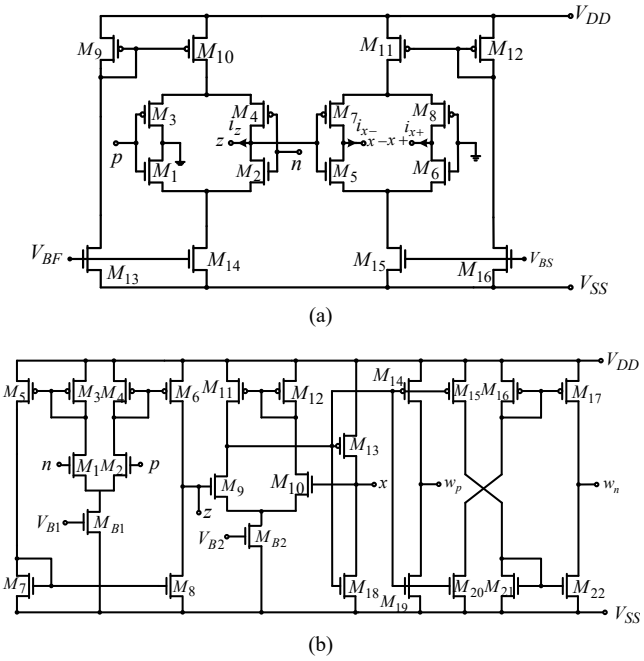


Fig. 2. (a) CMOS implementation of VDTA. (b) CMOS implementation of VDCC.

primarily determined by the transconductance of the output transistors. A reasonable approximation for these gains can be given by:

$$\begin{aligned} g_{\mathrm{mF}} &\cong \left(\frac{g_1 g_2}{g_1+g_2}\right)+\left(\frac{g_3 g_4}{g_3+g_4}\right) \\ &= \sqrt{\mu_{\mathrm{n}} C_{\mathrm{oxn}} \left(W/2L\right)_{13}} \left(V_{\mathrm{BF}} - V_{\mathrm{SS}} - V_{\mathrm{Tn}}\right) \\ &\quad \left(\frac{\sqrt{\mu_{\mathrm{n}} C_{\mathrm{oxn}} \left(W/L\right)_1 \left(W/L\right)_2}}{\sqrt{\left(W/L\right)_1}+\sqrt{\left(W/L\right)_2}} + \frac{\sqrt{\mu_{\mathrm{p}} C_{\mathrm{oxp}} \left(W/L\right)_3 \left(W/L\right)_4}}{\sqrt{\left(W/L\right)_3}+\sqrt{\left(W/L\right)_4}}\right), \\ g_{\mathrm{mF}} &\cong K_{\mathrm{F}} \left(V_{\mathrm{BF}} - V_{\mathrm{SS}} - V_{\mathrm{Tn}}\right), \\ g_{\mathrm{mS}} &\cong \left(\frac{g_5 g_6}{g_5+g_6}\right)+\left(\frac{g_7 g_8}{g_7+g_8}\right) \\ &= \sqrt{\mu_{\mathrm{n}} C_{\mathrm{oxn}} \left(W/2L\right)_{16}} \left(V_{\mathrm{BS}} - V_{\mathrm{SS}} - V_{\mathrm{Tn}}\right) \\ &\quad \left(\frac{\sqrt{\mu_{\mathrm{n}} C_{\mathrm{oxn}} \left(W/L\right)_5 \left(W/L\right)_6}}{\sqrt{\left(W/L\right)_5}+\sqrt{\left(W/L\right)_6}} + \frac{\sqrt{\mu_{\mathrm{p}} C_{\mathrm{oxp}} \left(W/L\right)_7 \left(W/L\right)_8}}{\sqrt{\left(W/L\right)_7}+\sqrt{\left(W/L\right)_8}}\right), \\ g_{\mathrm{mS}} &\cong K_{\mathrm{S}} \left(V_{\mathrm{BS}} - V_{\mathrm{SS}} - V_{\mathrm{Tn}}\right). \end{aligned} \quad (2)$$

In the equation provided, μ represents the effective carrier mobility, C_{ox} denotes the gate-oxide capacitance per unit area, W and L represent the effective channel width and length of the i-th MOS transistor, and K_i corresponds to the gain factor of the Arbel-Goldminz cells. It is important to note that the AG cells employed in this configuration do not introduce additional imperfections in terms of voltage and current gain, unlike certain other active blocks such as current-conveyers [33]. These alternative active blocks are

often constrained by limitations in slew rate, bandwidth, and dynamic ranges. The VDTA based on AG cells exhibits the ability to drive a grounded load using a bipolar signal and maintains a feedback current that matches the output current across a wide frequency range. Consequently, the temperature dependence of the VDTA is influenced by the temperature-dependent nature of g_m, which is contingent upon the absolute magnitude of V_{Th} (threshold voltage). Notably, the approximate absolute change in V_{Th} is approximately −2.4 mV/°C. The temperature dependence of mobility, expressed as $\mu(T) = \mu(T_0)\,(T/T_0)^{-1/5}$, reveals a decrease in mobility by approximately 1.5% with increasing temperature, whereas the threshold voltage decreases by approximately 0.24%. It is evident that the decrease in mobility dominates the reduction in g_{mF} and g_{mS} as the temperature rises.

The configuration depicted in Fig. 1(a) indicates that the control voltage V_{BS} is determined by the voltage across the capacitance C_2. Based on the relationship defined in (1), we can derive the expression for the voltage across the external capacitor C_1 as follows:

$$v_{C_1}(t) = v_z(t) = \frac{\beta_F g_{mF}}{C_1}\int v_{in}(t)\,dt = \frac{\beta_F g_{mF}}{C_1}\varphi_{in}(t). \quad (3)$$

In the provided equation, $\varphi_{in}(t)$ represents the flux of the input voltage signal. The voltage v_{c1} is supplied to the V-to-I converter, which consists of transistors M_P-M_N. The resulting output current, denoted as i_{out}, can be determined by the following expression:

$$i_{out}(t) = g_{m0} v_{C_1}(t) = \frac{\beta_F g_{m0} g_{mF}}{C_1}\varphi_{in}(t). \quad (4)$$

The transconductance of the V-to-I converter is denoted as g_{m0}. As a result, the voltage across the capacitor C_2 can be expressed as follows:

$$v_{C_2}(t) = \frac{\beta_F g_{mF} g_{m0}}{C_1 C_2}\int \varphi_{in}(t)\,dt = \frac{\beta_F g_{mF} g_{m0}}{C_1 C_2}\rho_{in}(t) = V_{BS}. \quad (5)$$

The integral of flux, represented as $\rho_{in}(t)$, is involved in the equation. Equation (2) establishes that the voltage V_{BS} determines the transconductance g_{mS}.

$$g_{mS}(t) = K_S\left[\frac{\beta_F g_{mF} g_{m0}}{C_1 C_2}\rho_{in}(t) - V_{SS} - V_{Tn}\right]. \quad (6)$$

Considering the interconnection between the output ports $x+$ and $x-$ of the VDTA with the input ports, we can express the relationship as follows:

$$\begin{aligned} i_{in}(t) &= \pm i_{x-}(t) = \pm\beta_S g_{mS} v_z(t) \\ &= \pm\beta_S K_S\left[\frac{\beta_F g_{mF} g_{m0}}{C_1 C_2}\rho_{in}(t) - V_{SS} - V_{Tn}\right]\frac{\beta_F g_{mF}}{C_1}\varphi_{in}(t). \end{aligned} \quad (7)$$

The polarity of the derived relationship is contingent upon the switch position, either in position *a* or *b*, thereby allowing the definition of the direct or inverse mode of operation for the meminductor emulator circuits under consideration. Consequently, the equivalent inverse meminductance of the proposed floating emulator circuits controlled by flux can be expressed as follows:

$$L_M^{-1}(t) = \pm\frac{\beta_F\beta_S g_{mF} K_S}{C_1}\left[\frac{\beta_F g_{mF} g_{m0}}{C_1 C_2}\rho_{in}(t) - V_{SS} - V_{Tn}\right]. \quad (8)$$

The derived equation (8) highlights that the meminductor emulator presented introduces the control transconductance parameters g_{mF} and g_{m0} of the VDTA and V-I converter, in addition to the frequency and amplitude values of the input voltage across its terminals. This feature provides an additional control parameter to adjust the area of the pinched hysteresis loop. Moreover, it enables the attainment of a smooth pinched hysteresis loop at high frequencies, without necessitating any changes to the frequency and amplitude of the input signal.

The memcapacitive emulator (MCI) configuration is illustrated in Fig. 1(b). It encompasses two grounded capacitors, an electronically controlled resistor (R_{eq}), and a voltage-to-current (V-I) converter in the second stage. The terminal characteristics of the Voltage Differencing Current Conveyor (VDCC) [35], illustrated in Fig. 1(b), can be described by the hybrid matrix, as defined by (9):

$$\begin{bmatrix} i_n \\ i_p \\ i_z \\ v_x \\ i_{w_p} \\ i_{w_n} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta g_m & -\beta g_m & 0 & 0 \\ 0 & 0 & \gamma & 0 \\ 0 & 0 & 0 & \alpha_p \\ 0 & 0 & 0 & -\alpha_n \end{bmatrix}\begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \end{bmatrix}. \quad (9)$$

The VDCC demonstrates high impedance across all terminals, except for the *x* terminal. In this context, β denotes the tracking error of the OTA stage of the VDCC, ideally taking the value of 1. The non-ideal voltage gain between the *z* and *x* terminals is represented by γ, with an ideal value of 1. Furthermore, α_p and α_n respectively indicate the non-ideal current gain between the *x*, w_p, and w_n terminals, ideally equaling 1. The transconductance gain of the VDCC can be calculated using the following expression:

$$g_m = k(V_{B1} - V_{Tn} - V_{SS}) \quad (10)$$

where

$$k = B\mu_{nB}C_{oxB}\sqrt{\frac{1}{2}\left(\frac{W}{L}\right)_{MB1}\left(\frac{W}{L}\right)_{MN}}. \quad (11)$$

The ratio $(W/L)_{MN}$ is defined as $(W/L)_{M1} = (W/L)_{M2}$, and the current mirroring ratio between transistors M_3, M_4, M_5, and M_6 is denoted as *B*. Additionally, μ_{nB} represents the electron mobility and C_{oxB} represents the oxide gate capacitance per unit area of the M_{B1} transistor. Examining (9), we observe that the *p, n*, and *z* terminals function as

a transconductance amplifier, while the other ports (x, w_p, and w_n), including the output z of the first stage, are connected to the internal current conveyor stage. These two stages can be implemented using CMOS technology, as demonstrated in Fig. 2(b) [35], with a total of 24 MOS transistors.

The equivalent resistance R_{el}, which is realized by two p-MOS transistors in Fig. 1(b), between the selected node of the VDCC and ground can be adjusted by a control voltage V_c. This relationship is defined as follows:

$$R_{el} = \frac{1}{2\mu_p C_{ox}\left(V_c - V_{Tp}\right)}\left(\frac{1}{W/L}\right)_{MR}. \tag{12}$$

The ratio $(W/L)_{MR}$ is defined as $(W/L)_{MR1} = (W/L)_{MR2}$. In the high-frequency region, instead of the grounded capacitances shown in Fig. 1, MOS-capacitances can be utilized in the emulator circuits, which offers additional advantages in terms of integrated circuit implementation.

The emulation of the floating memcapacitor is a highly intricate task, and a compact realization as proposed in this work is unprecedented in the existing literature. Analyzing the circuits depicted in Fig. 2(b), we can infer, based on the functional relationships among the ports of the VDCC, the following conclusions:

$$\begin{aligned}
&i_{W_p} = -i_{W_n} = \alpha_p i_x = i_{in} \Rightarrow \\
&\quad v_x(t) = \frac{1}{\alpha_p C_1}\int_0^t i_{in}(t)\,\mathrm{d}t = \frac{1}{\alpha_p C_1} q(t), \\
&i_{out}(t) = g_{m0} v_x(t) \Rightarrow \\
&\quad V_B(t) = \frac{1}{C_2}\int_0^t i_{out}(t)\,\mathrm{d}t = \frac{g_{m0}}{\alpha_p C_1 C_2}\int_0^t q(t)\,\mathrm{d}t = \frac{g_{m0}}{\alpha_p C_1 C_2}\sigma(t)
\end{aligned} \tag{13}$$

where $\sigma(t)$ is time integral of charge. It follows:

$$\begin{aligned}
&i_z = \pm\beta g_m\left(v_{in+} - v_{in-}\right) = \\
&\quad \pm\beta k\left(V_B(t) - V_{Tn} - V_{SS}\right)\left(v_{in+} - v_{in-}\right), \\
&v_z = R_{el} i_z = \frac{v_x}{\gamma} = \frac{1}{\alpha_p \gamma C_1} q(t) \Rightarrow \\
&\pm\beta k R_{el}\left(V_B(t) - V_{Tn} - V_{SS}\right)\left(v_{in+} - v_{in-}\right) = \frac{1}{\alpha_p \gamma C_1} q(t) \Rightarrow \\
&\left(v_{in+} - v_{in-}\right) = \\
&\quad \pm\frac{1}{\beta k R_{el}\left(\frac{g_{m0}}{\alpha_p C_1 C_2}\sigma(t) - V_{Tn} - V_{SS}\right)\alpha_p \gamma C_1} q(t).
\end{aligned} \tag{14}$$

Consequently, the resulting equivalent memcapacitance can be expressed as:

$$C_M^{-1} = \pm\frac{1}{\beta k R_{el}\left(\frac{g_{m0}}{\alpha_p C_1 C_2}\sigma(t) - V_{Tn} - V_{SS}\right)\alpha_p \gamma C_1}. \tag{15}$$

By selecting the appropriate port of the VDCC to which the input voltage of the proposed emulation circuit is connected (through the positioning of switches SW1 and SW2), the shape of the memcapacitor characteristic can be determined. This choice determines whether the pinched hysteresis loop will pass through quadrants 1 and 3 (direct memcapacitance) or quadrants 2 and 4 (inverted memcapacitance, also known as negative memcapacitance). Furthermore, the proposed emulator circuits depicted in Fig. 2(b) offer the flexibility of soft or hard switching. The mode of switching depends on the placement of breakpoints on the pinched hysteresis loop, which are influenced by the moment when the charge on the emulator circuits reaches its maximum value, such as when the input current signal reaches zero-crossing. Assuming the input current is defined as $I_m\cos(\omega t)$ and considering that the voltage value converges to zero, the resulting transient characteristic tends towards the q-axis, enabling a hard switching characteristic (the maximum charge occurs when the excitation current reaches its peak value and the charge integral approaches zero). Based on this, the value of the input voltage at the moment when there is a change in the direction of the operating point's movement on the transient characteristic can be defined as:

$$\begin{aligned}
&v(t_1) = \mp\frac{I_m}{\alpha_p \beta\gamma k R_{el}\left[V_{SS} + V_{Tn}\right]\omega C_1} \to 0, \\
&\frac{\omega\alpha_p \beta\gamma k R_{el} C_1}{I_m}\left[V_{SS} + V_{Tn}\right] >> 1.
\end{aligned} \tag{16}$$

By analyzing the obtained condition, it becomes apparent that adjusting the frequency of the current excitation signal or modifying the capacitance value allows for changes in the switching characteristics, particularly the width of the pinched hysteresis loop (PHL). Furthermore, by selecting the appropriate input voltage connection, it is also feasible to realize the characteristic of an inverting memcapacitance. The emulator circuits, which exhibit hard switching behavior, find application in circuits such as spiking and bursting neuron circuits, and they effectively exhibit two states: high and low memcapacitance. It is possible to switch the circuit to inverse operation by establishing a functional relationship between the input voltage and the charge, thereby facilitating an incremental mode of operation. In the direct mode, the memcapacitor emulator functions in a decremental mode. In the incremental mode, the value of the memcapacitance increases from the initial negative value, as indicated by (15).

3. Non-ideal and Parasitic Analysis

In practical scenarios, the VDTA and VDCC experience non-ideal gains, referred to as tracking errors, as discussed in the previous section of this paper. These tracking factors remain consistent and independent of frequency within the low to medium frequency ranges. Analyzing the relationships presented in (8) and (15), we observe that the proposed designs exhibit magnitudes of sensitivity values,

where the normalized passive and active sensitivities are equal to or less than unity in magnitude. Consequently, we can infer that the proposed circuits offer low passive and active sensitivities.

The presence of parasitic resistances and capacitances is observed in parallel with the corresponding terminals (*p, n, z, x+* and *x−*) of the VDTA. In an ideal VDTA, these parasitic resistances approach infinity, while the parasitic capacitances approach zero. However, in practical scenarios, they manifest as a shunt *R*-*C* network in conjunction with external circuit elements. Considering the influence of these parasitic components, including the parasitic capacitance, on the V-I converter output ($C_{\text{V-I}}$), we can analyze the operation of the proposed meminductor emulator in high-frequency environments. At high frequencies, the impact of R_{z}, $R_{\text{x+}}$, $R_{\text{x–}}$, R_{p} and $R_{\text{x–}}$ can be neglected. Hence, we can conclude that:

$$L_{\text{M}}^{-1}(t) = \pm\frac{\beta_{\text{F}}\beta_{\text{S}}g_{\text{mF}}K_{\text{S}}}{(C_1+C_{\text{z}})}\left[\frac{\beta_{\text{F}}g_{\text{mF}}g_{\text{m0}}}{(C_1+C_{\text{z}})(C_2+C_{\text{V–I}})}\rho_{\text{in}}(t)-V_{\text{SS}}-V_{\text{Tn}}\right]. \tag{17}$$

Considering the presence of parasitic capacitances at ports *p* and *x–*, the current-voltage relationship defined by (6) can be modified to take the following form:

$$i_{\text{in}}(t) = \pm\frac{\beta_{\text{F}}\beta_{\text{S}}g_{\text{mF}}K_{\text{S}}}{(C_1+C_{\text{z}})}\left[\frac{\beta_{\text{F}}g_{\text{mF}}g_{\text{m0}}}{(C_1+C_{\text{z}})(C_2+C_{\text{V–I}})}\rho_{\text{in}}(t)-V_{\text{SS}}-V_{\text{Tn}}\right]\varphi_{\text{in}}(t)+\left(C_{\text{p}}+C_{\text{x–}}\right)\frac{\text{d}v_{\text{in}}(t)}{\text{d}t}. \tag{18}$$

Equation (18) still represents a meminductor, with the additional effect of a total capacitance $C_{\text{p}}+C_{\text{x–}}$ connected in parallel with the input port. The second term in (18) accounts for the impact of this parasitic capacitance. This effect can manifest as a shift in the pinched-hysteresis loop on the flux-current characteristics, deviating the pinch-off point from the origin. However, in practical scenarios, this effect can be nullified by connecting a small capacitance with an appropriate value in parallel to the emulator circuit.

At the corresponding terminals *p*, *n*, *z*, w_{p}, and w_{n}, there are parasitic resistances R_{p}, R_{n}, R_{z}, R_{wp} and R_{wn}, as well as parasitic capacitances C_{p}, C_{n}, C_{z}, C_{wp} and C_{wn} (in an ideal VDCC, these parasitic resistances are approximately infinite, and the parasitic capacitances are approximately zero). Furthermore, at the port *x*, there exists a parasitic resistance R_{x} and a parasitic inductance L_{x} in series (in an ideal VDCC, R_x and L_{x} are approximately zero). Considering the influence of these parasitic elements, the equivalent memcapacitance of the emulator circuits depicted in Fig. 1(b) can be defined as:

$$C_{\text{M}}^{-1} = \pm\frac{1+sR_{\text{el}}C_{\text{z}}}{\beta k R_{\text{el}}\left(\frac{g_{\text{m0}}}{\alpha_{\text{p}}C_1(C_2+C_{\text{V–I}})C_2}\sigma(t)-V_{\text{Tn}}-V_{\text{SS}}\right)\alpha_{\text{p}}\gamma C_1}. \tag{19}$$

Based on the derived relations (17) to (19), it is crucial to select external capacitors C_1 and C_2 with values several times higher than the parasitic capacitances of the corresponding ports they are connected to. This selection ensures effective absorption of parasitic capacitance effects at operating frequencies. To mitigate the impact of parasitic resistances, C_1 and C_2 should be chosen such that their equivalent impedance is several times smaller than the parasitic resistances of the VDTA and VDCC ports.

Furthermore, it is important to note that the transconductance of the OTA cell in both VDTA and VDCC is a frequency-dependent parameter. Its bandwidth limitation can be adequately described by a single pole model. Thus, the transconductance gain and the parameter *k* of the first stage of VDCC and both stages of VDTA can be defined as follows:

$$g_{\text{m}} = g_{\text{m0}}\frac{\omega_{\text{g}}}{(s+\omega_{\text{g}})};k = k_0\frac{\omega_{\text{k}}}{(s+\omega_{\text{k}})}. \tag{20}$$

In the given equations, the transconductance gain is represented by g_{m0}, and the gain factor of the OTA cell at zero frequency is denoted as k_0. The pole frequencies, $\omega_{\text{g}} = 1/\tau_{\text{g}}$ and $\omega_{\text{k}} = 1/\tau_{\text{k}}$, correspond to the respective delays τ_{g} and τ_{k}. These pole frequencies characterize the bandwidth limitations of the system. By substituting the values of g_{m} and *k* into (17) to (19), a more comprehensive understanding of the frequency characteristics of the emulators can be obtained, including their dependence on non-idealities. It is evident that the emulators depicted in Fig. 1 have a useful operating frequency range defined as $\omega << \min(\omega_{\text{g}}, \omega_{\text{k}})$. The specific values of these pole frequencies in (20) will depend on the practical implementation of the VDTA and VDCC. To enhance the bandwidth of the VDTA and VDCC, a compensating resistor *R* can be introduced at port *p*. This modification alters the transconductance gain, yielding a new value defined as $g_{\text{m}} = g_{\text{m0}}/(1+g_{\text{m0}}R)$. Consequently, the bandwidth of the OTA cell can be adjusted accordingly.

4. Simulation Results

The proposed MIE and MCE circuits were simulated using Cadence Virtuoso software, and their operational performance was analyzed using TSMC CMOS 0.18 μm process model parameters. In the internal structure of the proposed MIE (VDTA), the MOS transistors have aspect ratios of 13 μm/0.36 μm for pMOS transistors and 4 μm/0.36 μm for nMOS transistors [20], [39]. To ensure that M_{N} and M_{P} are in the saturation region and for proper V-to-I conversion, the DC supply voltages are selected as

±0.9 V. The power consumption of the proposed VDTA (Fig. 2(a)) is measured to be 0.62 mW.

In the case of the MCE configuration based on VDCC, the V_{B2} voltage is set to 0 V. The bulk terminals of pMOS and nMOS transistors are connected to their respective source terminals and the most negative voltage point (V_{SS}). The aspect ratios of VDCC transistors (Fig. 2(b)) are specified in Tab. 1 [35], with M_{B1}, M_{B2}, MR_1, and MR_2 chosen as 3.6 µm/1.8 µm, 3.06 µm/0.72 µm, 60 µm/2 µm, and 60 µm/2 µm, respectively. An electronic resistor, implemented using only two PMOS transistors, can be tuned by the control voltage. A control voltage of 0.65 V results in an equivalent resistance of $R_{el} = 1.47$ kΩ. The power consumption of the proposed VDCC (Fig. 2(b)) is measured to be 0.869 mW.

Transistor	W (µm)	L (µm)
M1–M4	3.6	1.8
M5, M6	7.2	1.8
M7, M8	2.4	1.8
M9, M10	3.06	0.72
M11, M12,	9	0.72
M13–M17	14.4	0.72
M18–M22	0.72	0.72

Tab. 1. Dimensions of the transistors – VDCC.

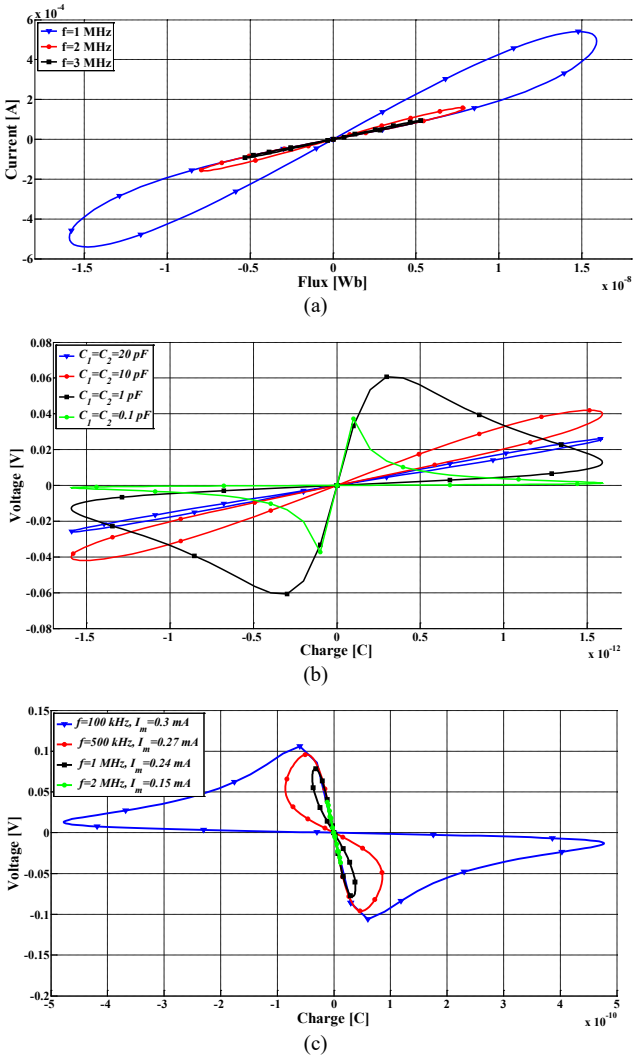


Fig. 3. Transient responses of the proposed emulator circuits: (a) The input current-flux relationship for proposed MIE for different frequencies, $C_1 = C_2 = 50$ pF; $V_{BS} = -0.31$ V. (b) MCE for different capacitances, $f = 10$ MHz. (c) for different frequencies and amplitude of the input current signal in inverting mode of operation, $C_1 = C_2 = 100$ pF.

During the simulation of transient characteristics of Meminductive Emulator (MIE) and Memcapacitive Emulator (MCE), a sinusoidal voltage/current signal with a varying frequency was utilized. The phase shift of the voltage signal was set to 90° frequency and an amplitude of $V_m = 100$ mV, while for the MCE, an input sinusoidal current signal with an amplitude of $I_m = 100$ µA was employed. Figure 3(a) plots clearly demonstrate the distinctive property of meminductivity. As the frequency increases, the pinched hysteresis becomes narrower, resulting in reduced lobes on the i-φ plane. The behavior of the lobes resembles an inclined number "8" passing through the origin. The decrease in the dynamic range of flux (x-axis) at higher frequencies can be attributed to the functional relationship derived from the emulated meminductance value (8). This functional relationship is influenced by the diminishing magnitude of the first term, which exhibits an inverse correlation with the frequency of the voltage signal being processed. This characteristic is not only dependent on the amplitude-to-frequency ratio of the exciting signal but also influenced by the capacitor value of the emulator circuit itself. By decreasing the capacitor value, the MIE can operate at higher frequencies. Figure 3(b) illustrates the simulation results of the proposed MCE at an excitation current signal frequency of 10 MHz, considering different values of ground capacitances C_1 and C_2. This analysis demonstrates the transition between different switching mechanisms. Decreasing the capacitance brings the bending point on the transient characteristic closer to the q-axis, causing the corresponding voltage value at that point to converge to zero, as predicted by theoretical analysis. Practically, increasing or decreasing the capacitor values results in a decrease or increase, respectively, in the area of the pinched hysteresis curve. This behavior arises due to the domination of the linear time-variant part over the linear time-invariant part of the memcapacitor, as described by (16). The same effect can be achieved by varying the frequency of the input current signal.

As predicted by theoretical analysis, the MCE can operate in an inverting mode (as well as MIE). To verify this operational regime, performance checks were conducted at different frequencies and amplitudes of the excitation signal, while maintaining a constant capacitance value ($C_1 = C_2 = 100$ pF) - as shown in Fig. 3(c). Based on the simulation results, it can be concluded that as the working frequency increases, the area covered by the lobes on the q-v plane decreases. Moreover, with an increase in the operating frequency, the pinched hysteresis curve area diminishes, causing the memcapacitor to behave more like an ordinary capacitor due to the decreasing contribution of the variable part in (15).

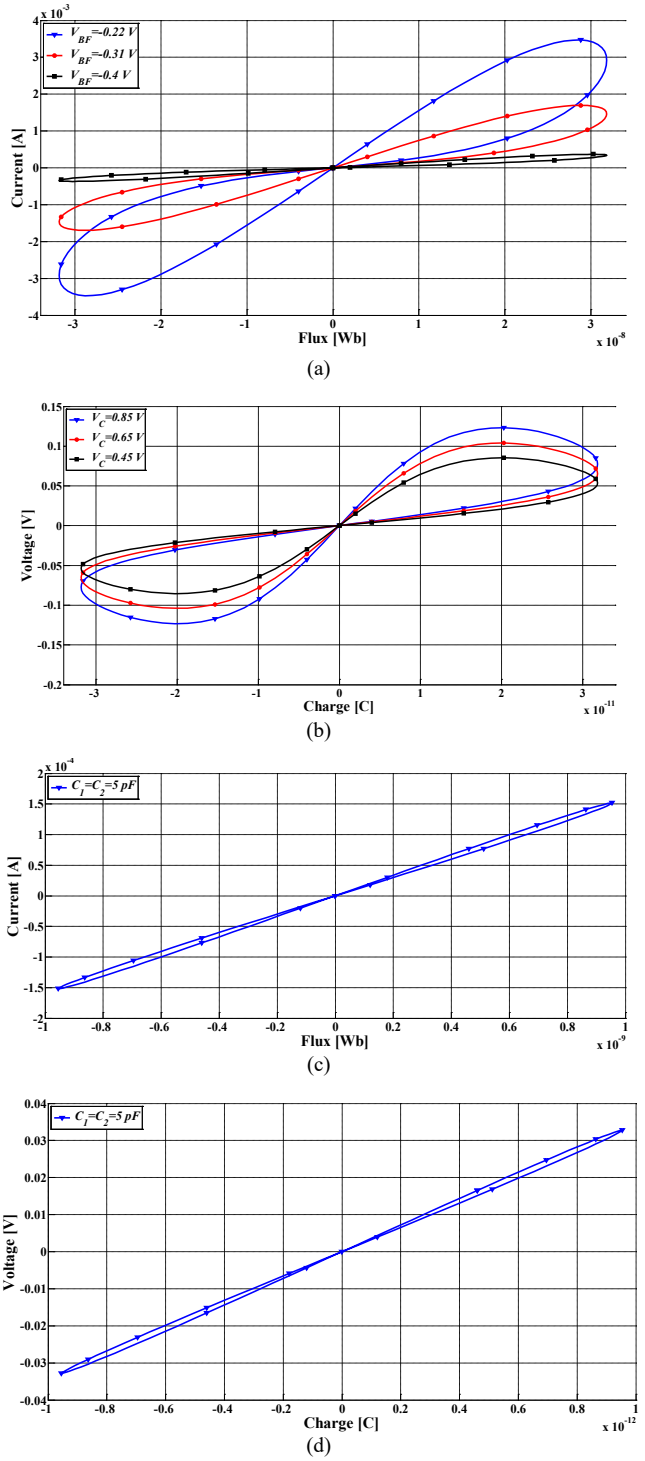
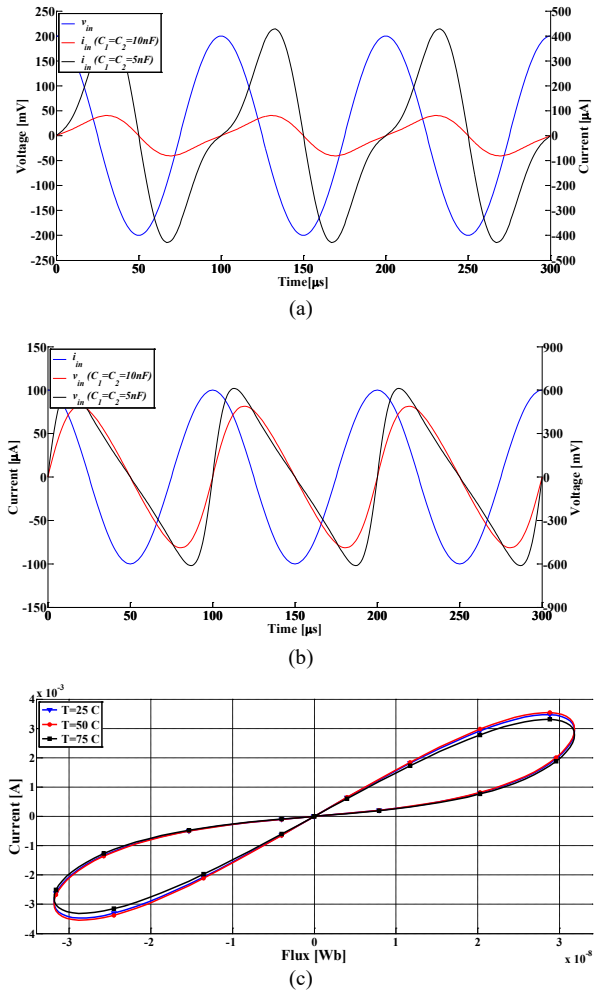
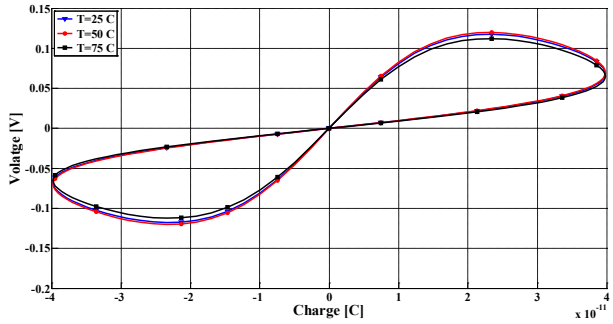


Fig. 4. (a) The input current-flux relationships for the different bias voltages of VDTA ($C_1 = C_2 = 50$ pF, $f = 1$ MHz, $V_m = 0.2$ V). (b) The input voltage-charge relationships for the proposed MCE for the different control voltage V_C. (c) Transient response of the proposed MIE for frequency of 50 MHz and amplitude $V_m = 300$ mV. (d) Transient response of the proposed MCE for frequency of 50 MHz and amplitude $I_m = 300$ µA.

The proposed MIE possesses an electronically adjustable feature, enabled by changing the transconductance parameter of the Voltage Differencing Transconductance Amplifier (VDTA), which allows for adjusting the flux value of the circuit. Figure 4(a) displays the input current-flux relationships of the proposed meminductor emulator for different bias voltages. Similarly, for the electronic control of MCE characteristics, the value of the control voltage (V_c) can be altered to adjust the charge of the circuit. Figure 4(b) exhibits the input charge-voltage relationships of the proposed memcapacitor emulator for different values of V_c, considering $C_1 = C_2 = 50$ pF, $f = 1$ MHz, and $I_m = 0.2$ mA. The maximum operating frequency of the emulated circuit proposed in Fig. 4(c) and (d) is limited to 50 MHz. This limitation arises from the practical limitations of the capacitance values achievable in the integrated technique. These capacitance values, specifically C_1 and C_2, are constrained by the size of the capacitors utilized, which in turn become comparable to the parasitic capacitances present on the VDTA and VDCC ports.

In order to demonstrate the transient characteristics of the proposed meminductor/memcapacitor emulators, a simulation is conducted using sinusoidal input voltage/current signals with a frequency of 10 kHz and amplitudes of 200 mV/100 µA, as depicted in Fig. 5. The current waveform (Fig. 5(a)) does not exhibit a sinusoidal shape due to the time-varying nature of the inductance value. As the frequency of the applied voltage signal increases, the phase difference between the input current and the flux value of the meminductor decreases.

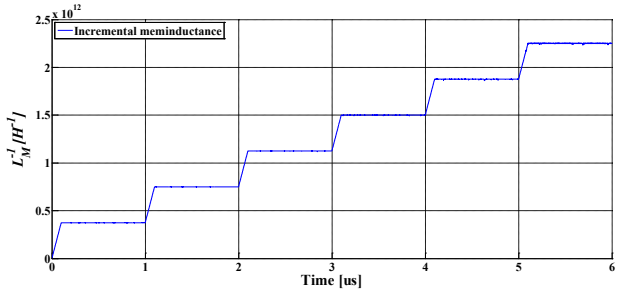




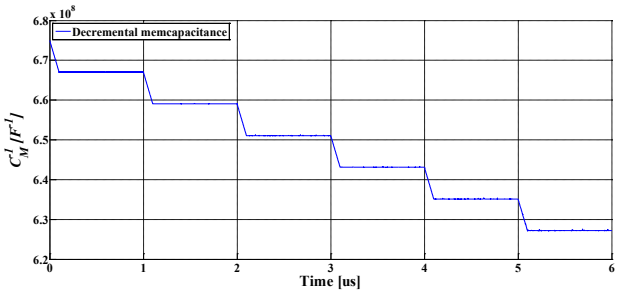
(d)

Fig. 5. (a) Time responses-time-domain response of the proposed MIE. (b) Time-domain response of the proposed MCE. (c) Hysteresis loop at various temperatures in MIE. (d) Hysteresis loop at various temperatures in MIE.

In Fig. 5(b) (proposed MCE), the generated voltage signal deviates from a sinusoidal waveform due to the time-varying nature of the memcapacitance. With an increase in the frequency of the input current signal, the phase difference between the input voltage signal and the charge value of the memcapacitance decreases. The temperature performance of the circuits illustrated in Fig. 1, is investigated through simulations conducted at three different temperature settings, as shown in Fig. 5(c) and (d). By examining the observed characteristics, it is evident that these circuits exhibit the anticipated properties across a broad temperature range ($C_1 = C_2 = 50$ pF, $f = 1$ MHz, $V_m = 0.2$ V/$I_m = 0.25$ mA, $V_{BF} = -0.22$ V). It is worth emphasizing that as the temperature decreases, there is an enhancement in the voltage/current flow within the meminductor/memcapacitor components.



(a)



(b)

Fig. 6. (a) Variation of meminductance with time in incremental configuration for the proposed MIE. (b) Variation of memcapacitance with time for the proposed MCE.

Moreover, an investigation into the non-volatile nature of the mem-system focuses on an important characteristic of MIE/MCE. To illustrate this feature, a pulse signal with a period of 1 µs, a pulse width of 0.1 µs, and an amplitude of 500 mV is applied to the proposed MIE (incremental mode) circuits depicted in Fig. 6(a) ($C_1 = 50$ pF, $C_2 = 85$ pF, $V_{BF} = -0.22$ V). Simulation results demonstrate the variation of meminductance over time. The ratio of current to flux changes during the ON time of the input pulse signal and remains constant during the OFF time, indicating that the meminductance increases when a voltage of the same value is occasionally applied. This behavior substantiates the non-volatile nature of the proposed meminductor. For the proposed MCE, a pulse input with an amplitude of 0.5 mA, a period of 1 µs, and a pulse width of 0.1 µs is utilized, while the external capacitance values are set as $C_1 = C_2 = 1$ nF. As evident from the simulation results presented in Fig. 6(b), the memcapacitance value remains constant even in the absence of a pulse signal, showcasing strong memory properties of the circuit between pulses. These configurations are practically suitable for the investigation and design of neuromorphic circuits incorporating synaptic plasticity, specifically long-term potentiation (LTP). In the field of neuroscience, LTP signifies the persistent strengthening of synapses based on recent patterns of activity, and it is considered a fundamental mechanism underlying learning and memory [40]. Additionally, by switching the proposed MCE circuit into the inverting mode, an incremental mode of operation can be achieved, as the memcapacitance value increases from the initial negative value, as described by (15).

4.1 Monte Carlo Simulation and Process Variation

The Monte Carlo (MC) simulations for the PHL curves of both realized meminductance (MI) and memcapacitor (MC) have also been presented. The plots have been shown here in Figs. 7(a) and 7(b) to describe the robustness nature of the proposed emulators. The MC simulations have generated for the 100 measurement samples for consideration of the overall process mismatch (10% tolerance) at frequency of 1 MHz. The slight deviation in the transient PHL loops can be observed between different curves plotted in Figs. 7(a) and 7(b), but overall the realized behaviors remain within acceptable limits. Figures 7(c) and 7(d) provide histograms of how the maximum values of the input current (for the proposed MIE) and voltage (for the proposed MCE) change, respectively.

The results indicate that the current flow in FF mode is larger than in SS mode, as expected. Despite the variation in the hysteresis loop area, all the proposed meminductor circuits exhibit a pinched hysteresis loop in all process corners. Furthermore, no offset is observed in the characteristics. If an offset were to appear in certain practical applications, compensation techniques can be employed. In our design, compensation can be achieved by adjusting the bias voltage of VDTA, which in turn compensates for the

operating point of the transistors. Further precise compensation can be accomplished through a more sophisticated internal structure of VDTA to reduce offset caused by leakage current and drift of the transistor's operating point. In summary, the proposed circuit can operate successfully across a wide range of temperatures and under different process corner conditions. For the proposed MCE, this study is performed at 10 MHz, with $C_1 = C_2 = 10$ pF and $I_m = 0.3$ mA – Fig. 8(b). Based on the simulation results, it is observed that the voltage/current flow in FF mode is larger than in SS mode, as expected, resulting in lower current flow in the SS process corner compared to the FF process corner. In conclusion, the proposed circuits can operate successfully across wide temperature ranges and under various process corner conditions.

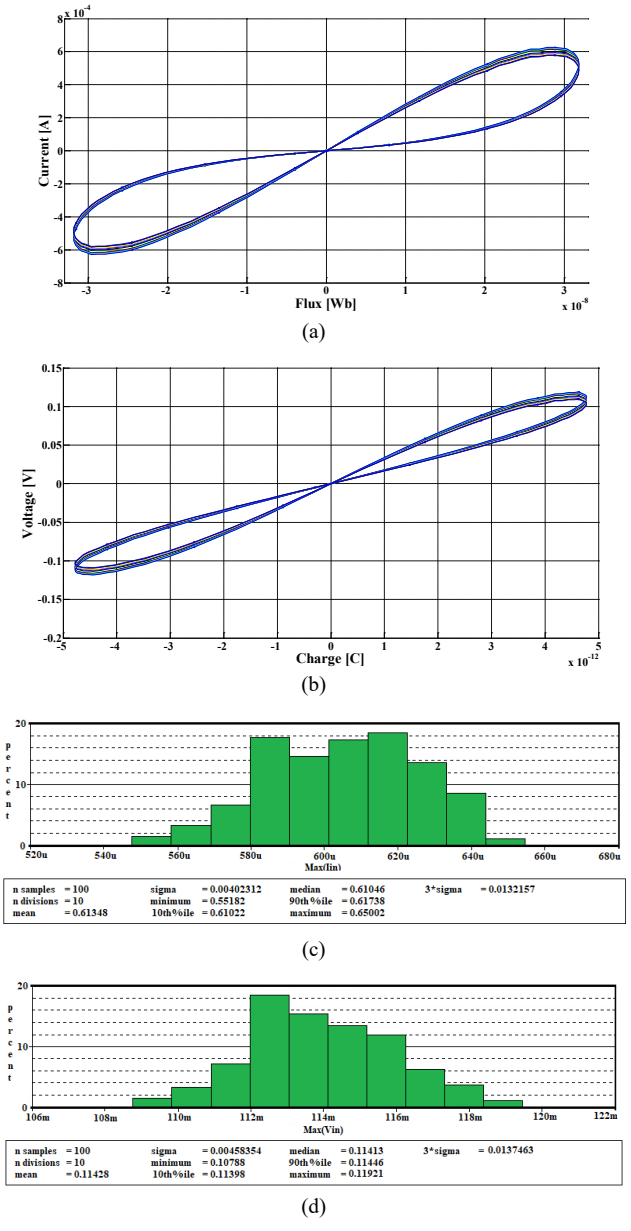


Fig. 7. Hysteresis loop of MC result (a) for MIE ($C_1 = C_2 = 50$ pF, $V_m = 0.2$ V); (b) for MCE ($C_1 = C_2 = 10$ pF, $f = 1$ MHz, $I_m = 0.3$ mA, $R_{el} = 1.47$ kΩ); (c) maximum point histogram for i_{in} values – MIE; (d) maximum point histogram for v_{in} values – MCE.

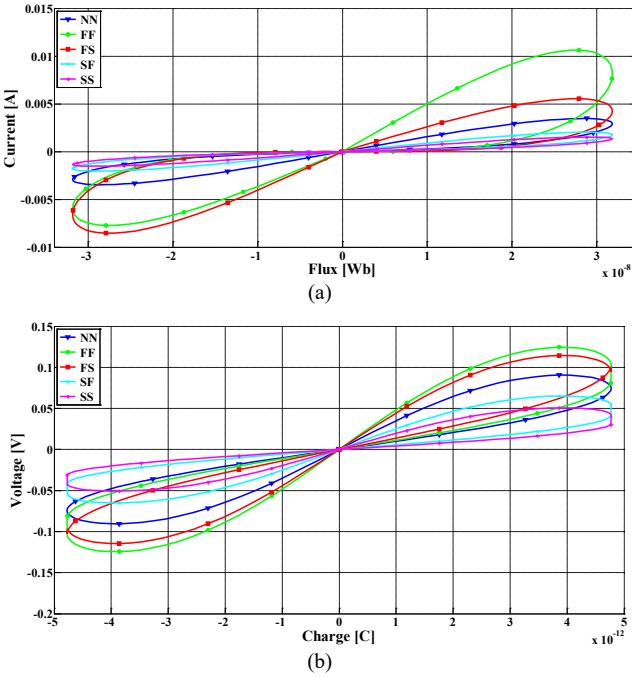


Fig. 8. Pinched hysteresis loop variation at different process corners: (a) MIE, (b) MCE.

4.2 Experimental Results

To better assess the practical performance of the proposed emulators, as the VDTA and VDCC components are not commercially available, the circuits depicted in Fig. 1 were constructed using readily available electronic devices. The prototype of the proposed MIE circuit was assembled on a breadboard using commercially accessible CA3080 ICs, illustrated in Fig. 9(a). The VDTA section was implemented using two CA3080 ICs, while the V-to-I section utilized a single CA3080 IC. Throughout the experiment, the CA3080 ICs were powered by a ±15 V DC power supply. The transconductance of the CA3080 could be controlled via biasing current, which was established using a biasing resistor ($R_A = 25$ kΩ) between a voltage and bias input terminal. The commercial IC-based implementation of VDCC followed the configuration proposed in [35], requiring the use of one LM13700 and one AD844, as shown in Fig. 9(b). Measurements were conducted using a Digilent Analog Discovery 2 board and probes. The amplitude of the input current signal ranged from $I_m = 0.4$ mA to $I_m = 0.6$ mA. In cases involving experimental validation of flux-controlled emulators, the input voltage signal had amplitudes of $V_m = 0.4$ V and $V_m = 0.5$ V.

The pinched hysteresis loops displayed in Figs. 9(c) and 9(d) were generated at operating frequencies of 20 kHz due to constraints imposed by available off-the-shelf devices and by reducing the value of capacitor C. At these frequencies, specialized compensation techniques or additional passive elements are not necessary. The measurement results obtained from the experimental setup closely resemble those from the simulation. Furthermore, it has been demonstrated that reducing the capacitor value brings the pinched hysteresis loop closer to the q-axis, indicating

a change in the switching mechanism. The resistance value of 100 Ω was substituted for R_{el}.

4.3 Comparison

Tables 2 and 3 provide a comprehensive comparison of various design and performance aspects between previously reported memelelements emulators and the proposed MIE/MCE in this study, focusing on recent developments in the field. The comparison encompasses multiple criteria, including the number of active and passive components, electronic tunability, frequency bandwidth, mode of operation, and power supply requirements. Based on the presented characteristics, it can be concluded that the proposed emulator circuits offer the highest operating frequency

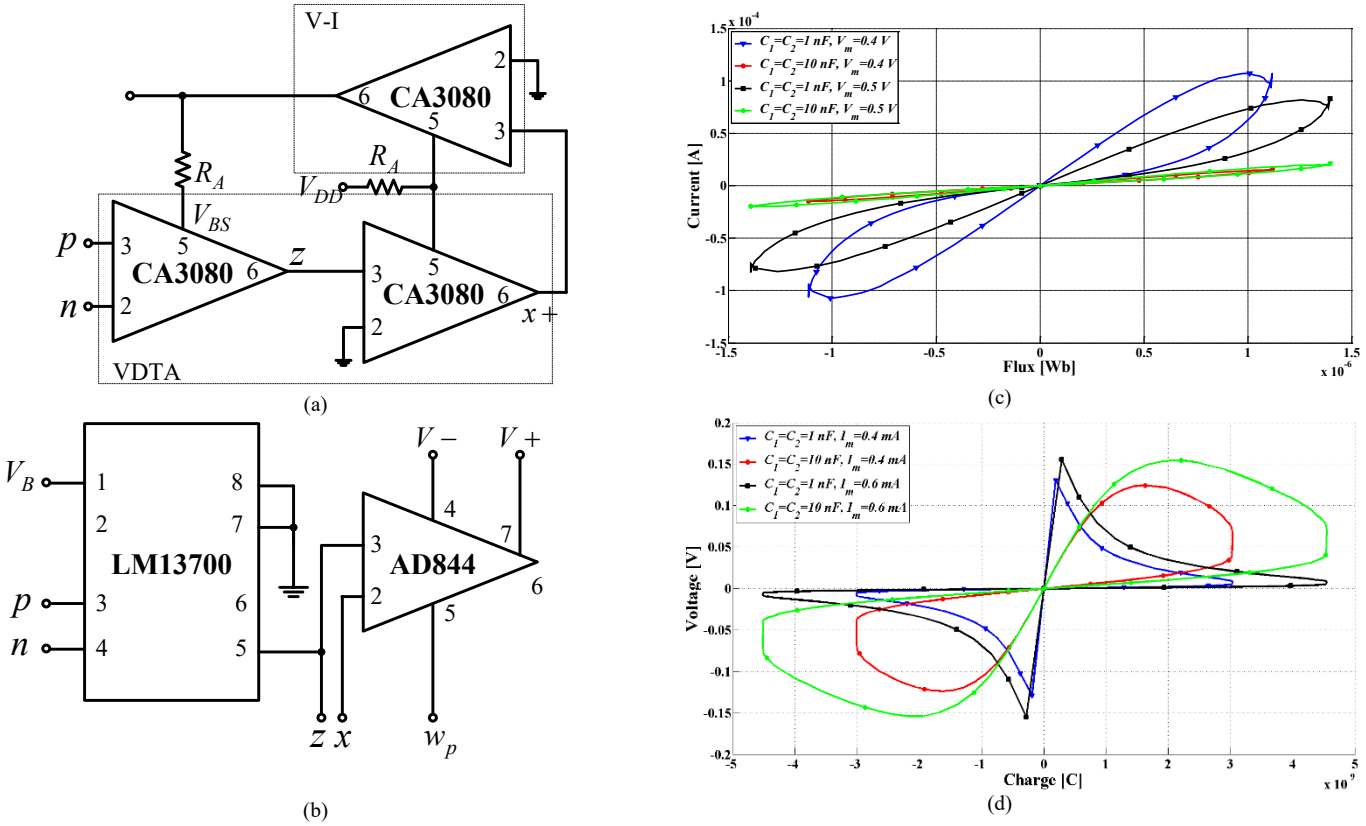


Fig. 9. (a) Practical implementation of VDTA and V-I. (b) Practical implementation of VDCC. (c) Experimental results of PHL for the proposed MIE. (d) Experimental results of PHL for the proposed MCE.

Ref.	Number of active comp.	Number of passive elements	Power supply	Maximum operating frequency	Type of emulator (F/G)	Electron. tunability	Need of external memristor
[9]	2 CBTA, 1 AM	2 R, 2 C	-	250 kHz	F	Yes	Yes
[10]	2 VDCC	1 R, 1 C	±0.9 V	700 kHz	G	No	Yes
[11]	2 CCII, 1 OTA	2 R, 2 C	±1.2 V	700 kHz	G	No	Yes
[12]	2 VDTA, 1 AM	1 R, 2 C	±0.9 V	1 MHz	G/F	Yes	No
[13]	2 OTA, 1 AM	2 R, 2 C	±1.25 V	10 kHz	G	Yes	No
[14]	3 OTA	2 C	±1.2 V	700 kHz	G	No	No
[15]	1 VDTA, 1 OTA	2 C	±1.2 V	3 MHz	G	Yes	No
[16]	2 VDTA	2 C	±0.9 V	1.5 MHz	F	Yes	No
[17]	2 VDCC, 1 AM, 2 MOSFETs	2 R, 1 C	±1.5 V	1.5 kHz	G	Yes	No
[18]	2 OTA, 1 CDBA	2 C	±0.9 V	2 MHz	G	Yes	No
[19]	1 MVDCC, 1 OTA	1 R, 2 C	±0.9 V	300 kHz	F	Yes	No
[20]	1 MO-VDTA	2 C	±0.9 V	50 MHz	F	Yes	No
[21]	1 VDBIA, 1 OTA, 2 MOS	2 C	±1 V	2 MHz	F	Yes	No
[22]	1 OTA, 1 CFOA, 2 CCII, 1 AM	8 R, 2 C	±15 V	5 kHz	F/G	Yes	No
[23]	1 DOCCII, 1 CCII, 1 AM	2 R, 2 C, 1 L	±12 V	700 kHz	G	No	No
[35]	2 VDCC	2 C	±0.9 V	50 MHz	F	Yes	No
This work	1 VDTA, 2 MOSFETs	2 C	±0.9 V	50 MHz	F	Yes	No

Tab. 2. Comparison of the exiting MIE with the proposed.

Ref.	Number of active comp.	Number of passive elements	Power supply	Maximum operating frequency	Type of emulator (F/G)	Electron. tunability	Need of external memristor
[24]	1 DXCCDITA	1 R, 2 C	±1.25 V	1 MHz	F	No	No
[25]	4 CFOA, 1 OA, 1 VD	5 R, 2 C	±15 V	10 kHz	F	No	No
[26]	2 CCII, 1 AM	4 R, 2 C	±10 V	25 kHz	F/G	No	No
[27]	2 VDCC	2 R, 2 C	±0.9 V	10 kHz	G	Yes	Yes
[28]	2 CCII, 1 AM	2 R, 2 C	±10 V	2 kHz	G	Yes	No
[29]	2 VDTA	2 C	±0.9 V	500 Hz	G	Yes	Yes
[30]	2 OTA, 1 UGA, 2 MOS capacitors	1 R	±15 V	24 MHz	F	Yes	No
[31]	1 VDTA	2 C	±0.9 V	50 MHz	G	Yes	No
[32]	1 FDCCII, 1 AM, 2 MOSFETs	3 C	±0.9 V	1 MHz	G	No	No
[33]	1 VDTA, 1 OTA, 1 Buffer	1 R, 3 C	±0.9 V	1.2 MHz	F	Yes	No
[34]	1 VDCC, 1 OTA	1 R, 2 C	±0.9 V	1 MHz	G	Yes	No
[35]	2 VDCC	1 R, 2 C	±0.9 V	2 MHz	G	Yes	No
This work	1 VDCC, 2MOSFETs	2C	±0.9 V	50 MHz	F	Yes	No

Tab. 3. Comparison of the exiting MCE with the proposed.

among all known circuits, while maintaining very low power consumption. Furthermore, the ability to electronically adjust the shape of the pinched hysteresis loops makes these emulators highly attractive for applications that necessitate compensation of parameter variations by manipulating their parameter values. Considering the parameters presented, the circuits described in this paper stand out for their simplicity and compact topology, wide bandwidth, and direct implementation potential as integrated circuits.

5. Conclusion

This paper presents a novel floating/grounded, incremental/decremental flux-controlled meminductor emulator circuit utilizing the VDTA active circuit element and two grounded capacitors. It also introduces a new structure for a current-mode floating charge-controlled memcapacitance emulator based on VDCC. These proposed configurations offer a simple and versatile design, featuring electrical tunability through bias voltage and a higher operating frequency range (up to 50 MHz) while utilizing fewer active and grounded passive elements compared to existing solutions. The simplicity of these circuits makes them compatible with other circuits, thereby extending the potential applications of mem-systems in the future. The effects of non-idealities in VDTA and VDCC, such as transfer gain errors and parasitic elements, on the realized memelement emulators are investigated. This analysis enables proper selection of passive circuit elements. Confirmation of the proposed concept (obtained based on theoretical assumptions and conclusions) was performed through simulation and experimental verification using off-shelf components. Various parameter variations, including process, capacitor, temperature, and frequency, are examined, with simulations demonstrating the capability to operate at frequencies up to 50 MHz. The proposed MCE circuit offers two switching mechanisms, namely soft and hard, depending on the capacitance value or the frequency of the input current signal. The paper establishes criteria defining the transition between these operating modes. Additionally, the circuit enables the simulation of a negative memcapacitance characteristic, which holds potential for nonlinear chaos oscillators and neuromorphic computing applications. To assess its performance, the proposed emulators are compared with existing solutions, showcasing superior performance in terms of power consumption, maximum operating frequency, and the number of active blocks required for integrated implementation. These improvements overcome limitations observed in previous implementations, enhancing the overall efficiency and applicability of the proposed circuits.

Acknowledgments

This research was supported by the Ministry of Education, Science and Technological Development of the Republic of Serbia, and these results are parts of the Grant No. 451-03-47/2023-01/200132 with University of Kragujevac - Faculty of Technical Sciences Čačak.

References

[1] CHUA, L. O. Memristor – The missing circuit element. *IEEE Transactions on Circuit Theory,* 1971, vol. 18, no. 5, p. 507–519. DOI: 10.1109/TCT.1971.1083337

[2] CHUA, L. O. Device modeling via nonlinear circuit elements. *IEEE Transactions on Circuits and Systems,* 1980, vol. 27, no. 11, p. 1014–1044. DOI: 10.1109/TCS.1980.1084742

[3] CHUA, L. O., KANG, S. M. Memristive devices and systems. *Proceedings of the IEEE,* 1976, vol. 64, no. 2, p. 209–223. DOI: 10.1109/PROC.1976.10092

[4] DI VENTRA, M., PERSHIN, Y.V., CHUA, L. O. Circuit elements with memory: Memristors, memcapacitors, and meminductors. *Proceedings of the IEEE,* 2009, vol. 97, no. 10, p. 1717–1724. DOI: 10.1109/JPROC.2009.2021077

[5] KHALIL, N. A., FOUDA, F. E., SAID, L. A., et al. A general emulator for fractional-order memristive elements with multiple pinched points and application. *AEU - International Journal of Electronics and Communications*, 2020, vol. 124, p. 1–15. DOI: 10.1016/j.aeue.2020.153338

[6] BIOLEK, D., BIOLEK, Z., BIOLKOVA, V. SPICE modeling of memristive, memcapacitative and meminductive systems. In *2009 European Conference on Circuit Theory and Design.* Antalya (Turkey), 2009, p. 249–252. DOI: 10.1109/ECCTD.2009.5274934

[7] BIOLEK, D., BIOLEK, Z., BIOLKOVA, V. Behavioral modeling of memcapacitor. *Radioengineering,* 2011, vol. 20, no. 1, p. 228 to 233. ISSN: 1210-2512

[8] BIOLEK, D., BIOLEK, Z., BIOLKOVA, V. PSPICE modeling of meminductor. *Analog Integrated Circuits and Signal Processing,* 2011, vol. 66, no. 1, p. 129–137. DOI: 10.1007/s10470-010-9505-5

[9] ÇAM TAŞKIRAN, Z. G., SAĞBAŞ, M., AYTEN, U. E., et al. A new universal mutator circuit for memcapacitor and meminductor elements. *AEU - International Journal of Electronics and Communications*, 2020, vol. 119, p. 1–11. DOI: 10.1016/j.aeue.2020.153180

[10] SINGH, A., RAI, S. K. VDCC-based memcapacitor/meminductor emulator and its application in adaptive learning circuit. *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*, 2021, vol. 45, no. 4, p. 1151–1163. DOI: 10.1007/s40998-021-00440-x

[11] RAJ, N., RANJAN, R. K., KHATEB, F., et al. Mem-elements emulator design with experimental validation and its application. *IEEE Access*, 2021, vol. 9, p. 69860–69875. DOI: 10.1109/ACCESS.2021.3078189

[12] VISTA, J., RANJAN, A. High frequency meminductor emulator employing VDTA and its application. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2020, vol. 39, no. 10, p. 2020–2028. DOI: 10.1109/TCAD.2019.2950376

[13] KONAL, M., KACAR, F. Electronically tunable meminductor based on OTA. *AEUE - International Journal of Electronics and Communications*, 2020, vol. 126, p. 1–9. DOI: 10.1016/j.aeue.2020.153391

[14] RAJ, A., KUMAR, K., KUMAR, P. CMOS realization of OTA based tunable grounded meminductor. *Analog Integrated Circuits and Signal Processing*, 2021, vol. 107, no. 2, p. 475–482. DOI: 10.1007/s10470-021-01808-z

[15] KUMAR, K., NAGAR, B. C. New tunable resistorless grounded meminductor emulator. *Journal of Computational Electronics*, 2021, vol. 20, no. 3, p. 1452–1460. DOI: 10.1007/s10825-021-01697-5

[16] BHARDWAJ, K., SRIVASTAVA, M. New electronically adjustable memelement emulator for realizing the behaviour of fully-floating meminductor and memristor. *Microelectronics Journal*, 2021, vol. 114, p. 1–15. DOI: 10.1016/j.mejo.2021.105126

[17] ORMAN, K., YESIL, A., BABACAN, Y. DDCC-based meminductor circuit with hard and smooth switching behaviors and its circuit implementation. *Microelectronics Journal*, 2022, vol. 125, p. 1–7. DOI: 10.1016/j.mejo.2022.105462

[18] YADAV, N., RAI, S. K, PANDEY, R. New high frequency memristorless and resistorless meminductor emulators using OTA and CDBA. *Sadhana*, 2022, vol. 47, no. 1, p. 1–18. DOI: 10.1007/s12046-021-01785-z

[19] BHARDWAJ, K., SRIVASTAVA, M. New grounded passive elements-based external multiplier-less memelement emulator to realize the floating meminductor and memristor. *Analog Integrated Circuits and Signal Processing*, 2022, vol. 27, p. 1–21. DOI: 10.1007/s10470-021-01976-y

[20] PETROVIC, P. B. A new electronically controlled floating/grounded meminductor emulator based on single MO-VDTA. *Analog Integrated Circuits and Signal Processing*, 2022, vol. 110, no. 1, p. 185–195. DOI: 10.1007/s10470-021-01946-4

[21] BHARDWAJ, K., SRIVASTAVA, M. Compact floating dual memelement emulator employing VDIBA and OTA: A novel realization. *Circuits, Systems and Signal Processing,* 2022, vol. 41, p. 5933–5967. DOI: 0.1007/s00034-022-02067-7

[22] SOZEN, H., CAM, U. A novel floating/grounded meminductor emulator. *Journal of Circuits, Systems and Computers*, 2020, vol. 29, no. 15. DOI: 10.1142/S0218126620502473

[23] KORKMAZ, M. O., BABACAN, Y., YESIL, A. A new CCII based meminductor emulator circuit and its experimental results. *AEU - International Journal of Electronics and Communications*, 2023, vol. 158, p. 1–9. DOI: 10.1016/j.aeue.2022.154450

[24] VISTA, J., RANJAN, A. Simple charge controlled floating memcapacitor emulator using DXCCDITA. *Analog Integrated Circuits and Signal Processing*, 2020, vol. 104, no. 1, p. 37–46. DOI: 10.1007/s10470-020-01650-9

[25] YU, D., ZHAO, X., SUN, T., et al. A simple floating mutator for emulating memristor, memcapacitor, and meminductor. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2020, vol. 67, no. 7, p. 1334–1338. DOI: 10.1109/TCSII.2019.2936453

[26] SHARMA, P. K., RANJAN, R. K., KHATEB, F., et al. Charged controlled mem-element emulator and its application in a chaotic system. *IEEE Access*, 2020, vol. 8, p. 171397–171407. DOI: 10.1109/ACCESS.2020.3024769

[27] KONAL, M., KACAR, F., BABACAN, Y. Electronically controllable memcapacitor emulator employing VDCCs. *AEU - International Journal of Electronics and Communications*, 2021, vol. 140, p. 1–7. DOI: 10.1016/j.aeue.2021.153932

[28] YESIL, A., BABACAN, Y. Electronically controllable memcapacitor circuit with experimental results. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2021, vol. 68, no. 4, p. 1443–1447. DOI: 10.1109/TCSII.2020.3030114

[29] HOSBAS, M. Z., KAÇAR, F., YESIL, A. Memcapacitor emulator using VDTA-memristor. *Analog Integrated Circuits and Signal Processing*, 2022, vol. 110, no. 2, p. 361–370. DOI: 10.1007/s10470-021-01974-0

[30] ANANDA, Y. R., SATYANARAYAN, G. S., TRIVEDI, G. An optimized MOS-based high frequency charge controlled memcapacitor emulator. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2022, vol. 12, no. 4, p. 793–803. DOI: 10.1109/JETCAS.2022.3221314

[31] PETROVIC, P. B. Electronically adjustable grounded memcapacitor emulator based on single active component with variable switching mechanism. *Electronics*, 2022, vol. 11, no. 1, p. 1–15. DOI: 10.3390/electronics11010161

[32] KORKMAZ, M. O., YESIL, A. FDCCII based new memcapacitor emulator circuit with electronically tunable. *Mühendislik Bilimleri ve Araştırmaları Dergisi*, 2023, vol. 5, no. 1, p. 127–134. DOI: 10.46387/bjesr.1259980

[33] ANANDA, Y. R., SATYANARAYAN, G. S., TRIVEDI, G. A high frequency MOS-based floating charge controlled memcapacitor emulator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2023, vol. 70, no. 3, p. 1189–1193. DOI: 10.1109/TCSII.2022.3221334

[34] BHARDWAJ, K., SRIVASTAVA, M. New multiplier-less compact tunable charge-controlled memelement emulator using grounded passive elements. *Circuits, Systems and Signal Processing*, 2022, vol. 41, p. 2429–2465. DOI: 0.1007/s00034-021-01895-3

[35] PETROVIĆ, P. B. A universal electronically controllable memelement emulator based on VDCC with variable configuration. *Electronics*, 2022, vol. 11, p. 1–23. DOI: 10.3390/electronics11233957

[36] ARBEL, A. F., GOLDMINZ, L. Output stage for current-mode feedback amplifiers, theory and applications. *Analog Integrated Circuits and Signal Processing,* 1992, vol. 3, p. 243–255. DOI: 10.1007/BF00276637

[37] BHARDWAJ, K., SRIVASTAVA, M. Compact charge-controlled memristance simulator with electronic/resistive tunability. *Journal of Circuits, Systems, and Computers*, 2022, vol. 31, no. 5, p 1–21. DOI: 10.1142/S0218126622500943

[38] PETROVIĆ, P. B. Charge-controlled grounded memristor emulator circuits based on Arbel-Goldminz cell with variable switching behaviour. *Analog Integrated Circuits and Signal Processing,* 2022, vol. 113, p. 373–381. DOI: 10.1007/s10470-022-02042-x

[39] PETROVIĆ, P. B. Single VDTA-based lossless and lossy electronically tunable positive and negative grounded capacitance multipliers. *Circuits, Systems and Signal Processing,* 2022, vol. 41, p. 6581–6614. DOI: 0.1007/s00034-022-02094-4

[40] COOKE, S. F., BLISS, T. V. P. Plasticity in the human central nervous system. *Brain,* 2006, vol. 129, p. 1659–1673. DOI: 10.1093/brain/awl082

About the Authors …

Mihajlo TATOVIĆ was born in Kragujevac, Serbia, on October 13, 1990. He graduated at the Faculty of Technical Sciences in Čačak, University of Kragujevac Serbia, as the best graduate student in the school year 2013/2014 at the study program Electrical and Computer Engineering, module: electrical power systems. He is currently student at PhD studies. His research interest fields are: digital and analog electronics, power electronics, microcontroller systems, embedded systems, industrial automation**.**

Predrag B. PETROVIĆ was born in Čačak, Yugoslavia, on January 26, 1967. He received the B.S.E.E. and M.Sc. degrees in Electrical Engineering from the University of Belgrade, Yugoslavia, in 1991 and 1994, respectively, and Ph.D. degree in the field of digital signal processing at the University of Novi Sad in 2004. His main interest is digital signal processing, microcontroller programming, power electronics, AD conversion, mathematics, and cryptology. He published more than 170 journals and conference papers, six university books, three international monographs and holds seven patents. He is the member of MENSA.