Unequal Single-Ended-to-Balanced Power Divider with Enhanced Input-Matching Bandwidth

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Abstract. *To reduce the circuit size of a single-ended-to-balanced power divider, a section of coupled line with a short-circuited terminal is applied. In this structure, two transmission zeros are generated, which realizes a wide input-matching bandwidth without extra absorbing branches. The enhanced input matching bandwidth can decrease the effect of the reflection wave power on the operation of the preceding active stage in the RF front end. Equations are derived to support the power transmission in a specific power division ratio. To verify the proposed structure, a single-ended-to-balanced power divider operating at 2.0 GHz is designed, fabricated, and measured. A wide matching bandwidth under −10 dB covers from 0.292 to 3.966 GHz with a fractional bandwidth (FBW) of 183.7%. Simulation and measurement results are in good agreement.*

Keywords

SETB power divider, enhanced input-matching bandwidth, out-of-phase, coupled line

1. Introduction

With high immunity to EM interference, differential circuits have been widely used in modern communication systems. Power dividers as key components in both balanced and single-ended communication systems are widely used [1–4]. For an easy connection between the balanced and single-ended ports, components with the single-ended-to-balanced (SETB) structure have been studied [5–8], in which the SETB power divider can realize the division of single-ended signal into two differential ones, can be used for the RF front end as shown in Fig. 1. Besides, a power divider with out-of-phase characteristics can provide differential processes in balanced circuits without an extra inverter. Moreover, compared with Balun, an out-of-phase power divider can provide feasible isolation performance.

Commonly, the out-of-phase characteristic required in SETB power divider is realized by two transmission paths with a $\lambda/2$ path difference [8], however, this structure has a large circuit footprint. Coupled lines are used to realize the SETB power dividers [9], [10]. A section of coupled line with two short-circuited terminals is used to generate 180° phase difference in [11], and a section of coupled line with one port short-circuited is used to realize 3-ports power transmission with the out-of-phase characteristics [12], [13]. Due to the usage of a coupled line, a compact structure can be obtained. However, the matching characteristic of the power dividers in [12] needs to improve. A $\lambda/4$ transmission line is applied in [13] to realize good port matching leading to a narrow impedance bandwidth. To increase the flexibility of dividing power in a specific ratio, unequal power dividers have been studied [14–16].

Except for the EM interference, the out-of-band reflected signal could cause additional unwanted intermodulation. Undesired RF-signal-power reflections could deteriorate the operation of the preceding active stage [17], such as the power amplified in Fig. 1. To decrease the effect of the out-of-band reflected signal, an additional branch with a resistor and paralleled stepped impedance stub is used in [17]. The resistors used in the branches can absorb the reflected wave power in a single-ended power divider with an 80% fractional input matching bandwidth. In [18] a new absorbing branch is used to enhance the input matching band of the power divider. However, these additional branches are bulky and difficult to integrate. Besides, the double-side parallel-strip line and the hybrid of microstrip (MS) and slotline (SL) structure, a wideband characteristic is realized in the SETB power dividers [19–22]. However, the hybrid structure of MS and SL needs a large circuit area.

To reduce the influence of undesired RF-signal-power reflections on the operation of the preceding active stage in the RF front end, an unequal SETB power divider is proposed. The contributions are summed up as follows:

- This structure can realize a high power division ratio according to the coupling coefficient.
- With two extra reflection zeros, this power divider can provide an ultra-wide matching bandwidth.
- Without extra absorbing branches, this power divider can decrease the influence of the undesired RF-signal-power reflections in a simple structure.

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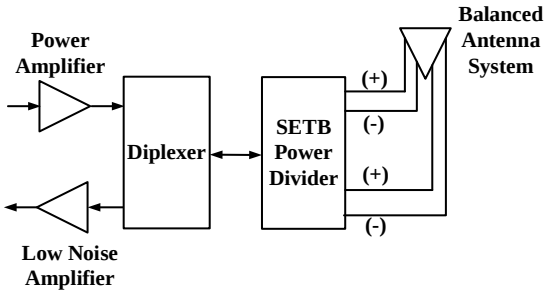

Fig. 1. SETB power divider for the RF front end.

2. Theory Analysis and Design

The topology of the proposed SETB power divider is shown in Fig. 2, which has one single-ended port 1, and two balanced ports A and B. Balanced ports A and B are composed of single-ended ports 2 and 3, 4, and 5, respectively. All ports are terminated with the port impedance Z_0. This power divider is composed of a coupled line with one short-circuited terminal, one resistor, two $\lambda/2$ transmission lines, and two $\lambda/4$ transmission lines.

The mixed-mode scattering parameters including the transmission coefficient of single-ended-mode, differential-mode, and common-mode are given as:

$$[S_{\mathrm{mm}}]=\begin{bmatrix} S_{ss11} & S_{sd1A} & S_{sd1B} & S_{sc1A} & S_{sc1B} \\ S_{dsA1} & S_{sd1B} & S_{ddAB} & S_{dcAA} & S_{dcAB} \\ S_{dsB1} & S_{ddBA} & S_{ddBB} & S_{dcBA} & S_{dcBB} \\ S_{csA1} & S_{cdAA} & S_{cdAB} & S_{ccAA} & S_{ccAB} \\ S_{csB1} & S_{cdBA} & S_{cdBB} & S_{ccBA} & S_{ccBB} \end{bmatrix}. \tag{1}$$

The equivalent circuit of coupled line is shown in Fig. 3.

The equivalent impedance Z_{eq1} and Z_{eq2} can expressed as given in [12] as

$$Z_{\mathrm{eq1}}=\frac{2Z_{\mathrm{e}}Z_{\mathrm{o}}}{Z_{\mathrm{e}}-Z_{\mathrm{o}}}, \tag{2}$$

$$Z_{\mathrm{eq2}}=\frac{2Z_{\mathrm{e}}Z_{\mathrm{o}}}{Z_{\mathrm{e}}+Z_{\mathrm{o}}} \tag{3}$$

where the Z_{e} and Z_{o} are the coupled line's even- and odd-mode characteristic impedances, respectively.

At the central frequency, when the power is transmitted into the output ports, the isolation resistor is considered short-circuited as shown in Fig. 4. Assume the power division ratio from port 1 to ports A and B is $1 : k^2$, then Z_{eq1} and Z_{eq2} are related as

$$k=\frac{Z_{\mathrm{eq1}}}{Z_{\mathrm{eq2}}}=\frac{Z_{\mathrm{e}}+Z_{\mathrm{o}}}{Z_{\mathrm{e}}-Z_{\mathrm{o}}}. \tag{4}$$

The power division ratio k is the reciprocal of the coupling coefficient of C. Because the coupling coefficient

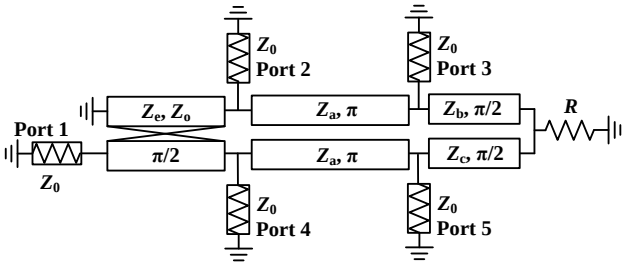

Fig. 2. Schematic of the proposed SETB power divider.

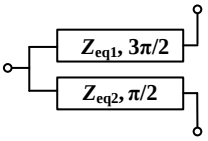

Fig. 3. Equivalent structure of the coupled line.

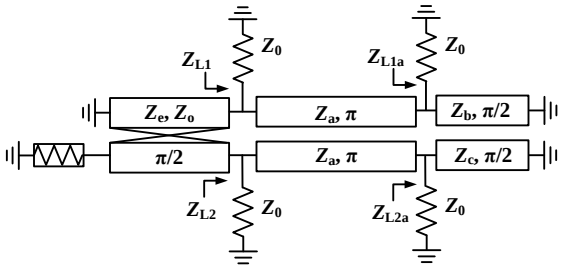

Fig. 4. Equivalent circuit with matching balanced ports.

of C is traditionally less than 1, the proposed structure can be used to realize unequal power division. The even- and odd-mode characteristic impedances can be expressed in terms of the power division ratio k as

$$Z_{\mathrm{e}}=Z_{01}\sqrt{(k+1)/(k-1)}, \tag{5}$$

$$Z_{\mathrm{o}}=Z_{01}\sqrt{(k-1)/(k+1)} \tag{6}$$

where Z_{01} is the equivalent of the coupled line.

Using the relation between voltage, current, and four-port coupled line with one port short-circuited and two ports terminated in the impedance Z_{L1} and Z_{L2}, respectively. The input conductance at the input port can be expressed as follows,

$$Y_{\mathrm{in}}=Y_{11}-\frac{Y_{31}Z_{\mathrm{L1}}}{1+Y_{33}Z_{\mathrm{L1}}} + \frac{\left(\begin{array}{l} Y_{31}{}^{2}Y_{34}{}^{2}Z_{\mathrm{L1}}/\left(1+Y_{33}Z_{\mathrm{L1}}\right)+Y_{41}{}^{2}\left(\dfrac{1}{Z_{\mathrm{L1}}}+Y_{33}\right) \\ -2Y_{14}Y_{31}Y_{34} \end{array}\right)}{Y_{34}Y_{43}-\left(\dfrac{1}{Z_{\mathrm{L2}}}+Y_{44}\right)\left(\dfrac{1}{Z_{\mathrm{L1}}}+Y_{33}\right)} \tag{7}$$

At the central frequency, the electrical lengths of the transmission lines are $\theta=\theta_2=\pi/2$ and $\theta_1=\pi$. The impedance Z_{L1} and Z_{L2} are given as follows,

$$Z_{\mathrm{L1}}=Z_0/2, \tag{8}$$

$$Z_{L2} = Z_0/2\,. \tag{9}$$

The *Y*-parameter of the four-port coupled line is given as follows [23],

$$Y_{11} = -\frac{\mathrm{j}}{2}\left(Y_\mathrm{e} + Y_\mathrm{o}\right)\cot\theta, \tag{10}$$

$$Y_{12} = -\frac{\mathrm{j}}{2}\left(Y_\mathrm{e} - Y_\mathrm{o}\right)\cot\theta, \tag{11}$$

$$Y_{13} = -\frac{\mathrm{j}}{2}\left(Y_\mathrm{e} - Y_\mathrm{o}\right)\csc\theta, \tag{12}$$

$$Y_{14} = -\frac{\mathrm{j}}{2}\left(Y_\mathrm{e} + Y_\mathrm{o}\right)\csc\theta \tag{13}$$

where $Y_\mathrm{e} = 1/Z_\mathrm{e}$, $Y_\mathrm{o} = 1/Z_\mathrm{o}$.

The input conductance can be simplified as

$$Y_\mathrm{in} = \frac{\left(Z_\mathrm{e}^2 + Z_\mathrm{o}^2\right)Z_0}{4Z_\mathrm{e}^2 Z_\mathrm{o}^2}. \tag{14}$$

The reflection coefficient is given as

$$\left|S_{11}\right| = \left|\frac{Y_\mathrm{in} - Y_0}{Y_\mathrm{in} + Y_0}\right|. \tag{15}$$

By substituting (5) and (6) into (22), the relation between the power division ratio and the return loss can be obtained as

$$\left|S_{11}\right| = \left|\frac{\left(\dfrac{k+1}{k-1} + \dfrac{k-1}{k+1}\right)Z_0^{\,2} - 4Z_{01}^{\,2}}{\left(\dfrac{k+1}{k-1} + \dfrac{k-1}{k+1}\right)Z_0^{\,2} + 4Z_{01}^{\,2}}\right|. \tag{16}$$

Once the power division ratio *k* is determined, a good input port matching can be obtained by choosing a proper Z_{01} according to (16).

As the above equations show, the impedance of the $\lambda/2$ transmission lines does not affect the central frequency ports matching. The combination of two $\lambda/2$ transmission lines and the coupled line with a short-circuited terminal can generate two reflection zeros, as shown in Fig. 5. The two reflection zeros are located at 0.3 and 1.7 times the central frequency, respectively. Hence, an enhanced matching bandwidth can be obtained. Compared with other cases the proposed structure can obtain a wider impedance bandwidth.

The impedance of the $\lambda/2$ transmission lines can affect the depth of the reflection zero points and the bandwidth of the input matching, a larger Z_a leads to a wider matching bandwidth. A larger Z_a leads to a narrower common-mode suppression (CMS) bandwidth at the same time, as shown in Fig. 6. Thus a tradeoff is required to choose the characteristics impedance of the $\lambda/2$ transmission lines.

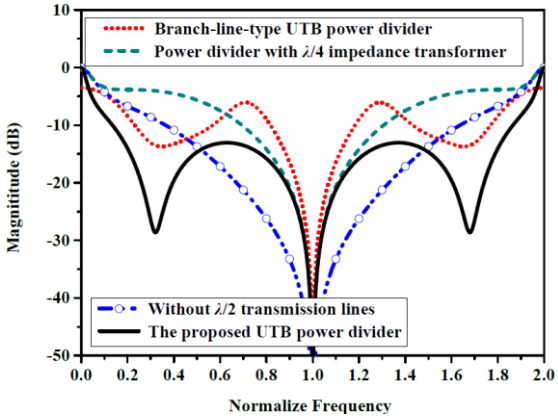

Fig. 5. Four cases impedance bandwidths.

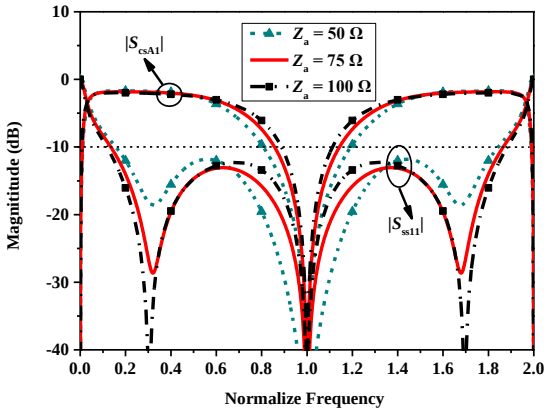

Fig. 6. Effect of the impedance of the two $\lambda/2$ transmission lines on input port matching.

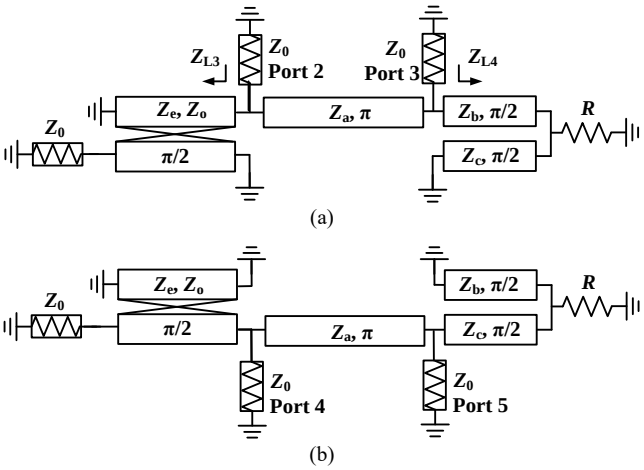

Fig. 7. Equivalent circuit of the power divider when different balanced ports excited: (a) Port B excited; (b) Port C excited.

To realize good isolation between the two output ports, no power should flow to port B when port A is excited. The equivalent circuit is given in Fig. 7(a) for this case.

The Y_{L3} and Y_{L4} in Fig. 7(a) are derived as

$$Y_{L3} = Y_{11} - \frac{Y_{13}Y_{31}}{Y_{11} + 1/Z_0} = \frac{\left(Y_\mathrm{e} - Y_\mathrm{o}\right)^2}{4Y_0}, \tag{17}$$

$$Y_{L4} = \frac{Z_b^2}{R}. \tag{18}$$

The *A*-matrix between ports 2 and 3 is given as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \dfrac{(Y_e - Y_o)^2}{4Y_0} & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \dfrac{R}{Z_b^2} & 1 \end{bmatrix}. \tag{19}$$

By converting the *A*-parameters into the *S*-parameters, the *S*-parameters for ports 2 and 3 can be derived as follows,

$$S_{23} = S_{32} = \frac{-8Z_b^2}{8Z_b^2 + \left[Z_0 Z_b^2 (Y_e - Y_o)^2 + 4R\right] Z_0}, \tag{20}$$

$$S_{22} = S_{33} = \frac{-\left[Z_0 Z_b^2 (Y_e - Y_o)^2 + 4R\right] Z_0}{8Z_b^2 + \left[Z_0 Z_b^2 (Y_e - Y_o)^2 + 4R\right] Z_0}. \tag{21}$$

The relation between the mixed-mode scattering parameter and the standard scattering parameter of balanced ports return loss is given as follows [24],

$$S_{ddAA} = \frac{1}{2}\left(S_{22} + S_{33} - S_{23} - S_{32}\right), \tag{22}$$

$$S_{ddBB} = \frac{1}{2}\left(S_{44} + S_{55} - S_{45} - S_{54}\right). \tag{23}$$

To realize a good matching of balanced ports, the conditions in equations need to meet $S_{ddAA} = S_{ddBB} = 0$. By setting the isolation resistor R as Z_0, the Z_b is derived as

$$Z_b = \sqrt{\frac{4RZ_0}{8 - Z_0^2 (Y_e - Y_o)^2}}. \tag{24}$$

Similarly, the Z_c can be derived and given as

$$Z_c = \sqrt{\frac{4RZ_0}{8 - Z_0^2 (Y_e + Y_o)^2}}. \tag{25}$$

The steps for the circuit design can be summarized as follows:

(1) Determine the required PDR k of the SETB power divider.

(2) Use (16) to obtain the equivalent impedance Z_{01}, and the even- and odd-mode characteristics Z_e and Z_o can be calculated using (5) and (6), respectively.

(3) Calculate the impedances Z_b and Z_c using (24) and (25) to realize good balanced ports matching.

(4) Choose a proper Z_a referring to Fig. 5 to make a tradeoff between the depth of the matching curve and the suppression bandwidth.

Four cases for different PDRs (i.e. 3, 6, 9, and 12 dB) are given in Tab. 1 using the above 4 steps with the isolation resistor R setting as 50 Ω.

k^2	Z_{01}	Z_e	Z_o	Z_b	Z_c
3 dB	61.5	148.72	25.43	43.26	60.86
6 dB	45.6	79.11	26.29	39.57	79.62
9 dB	40	57.96	27.6	37.53	108.47
12 dB	35.7	46.15	27.62	36.58	163.36

Tab. 1. Circuit parameters for different PDRs (unit: Ω).

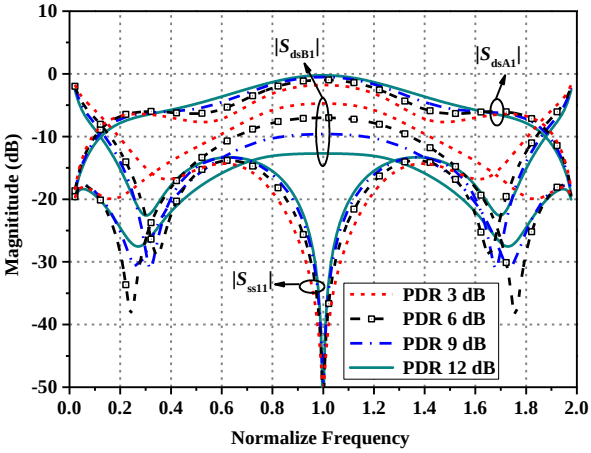

Fig. 8. Performances of four power dividers with different PDRs.

The simulation performances of 4 power dividers are given in Fig. 8. With the PDR increasing from 3 to 12 dB, these power dividers all have good input matching characteristics at the normalized central frequency with a wide −10-dB input matching fractional bandwidth (FBW).

As shown in Fig. 8, the weak coupling (Z_e = 46.15 Ω and Z_o = 27.62 Ω) provides a large PDR of 12 dB, and the tight coupling (Z_e = 148.72 Ω and Z_o = 25.43 Ω) realizes a small PDR of 3 dB. It can be found that a smaller PDR has a little narrower matching bandwidth.

3. Implementation and Performance

As a demonstration of the SETB power divider concept, a microstrip prototype was designed, fabricated, and measured at the central frequency f_0 2.0 GHz, with the performances and the specifications as the PDR of 10 dB, the circuit size less than 0.3 λ_g^2, the return loss larger than 20 dB, and the FBW of 180%. The relative permittivity and the thickness of the microwave substrate are ε_r = 2.65 ± 2%, and h = (1.5 ± 0.05) mm, respectively [25]. The electrical parameters of the SETB power divider are obtained using the design method in Sec. 2 as Z_0 = 50 Ω, Z_{01} = 39 Ω, Z_e = 54.11 Ω, Z_o = 28.11 Ω, Z_b = 37.09 Ω, and Z_c = 119.96 Ω. The final corresponding circuit dimensions are given in Tab. 2 by using the HFSS simulation software.

W_1	L_1	W_2	L_2	W_3	L_3	W_4	G
5.0	17.05	2.0	49.9	6.3	19.95	2.05	0.22

Tab. 2. Dimensions of the proposed power divider (unit: mm).

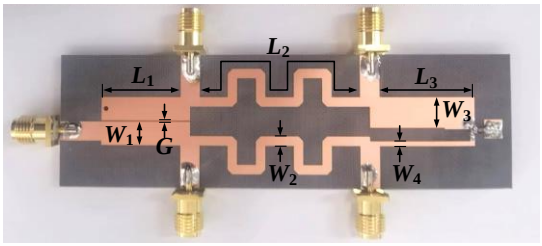

Fig. 9. Photograph of the proposed SETB power divider.

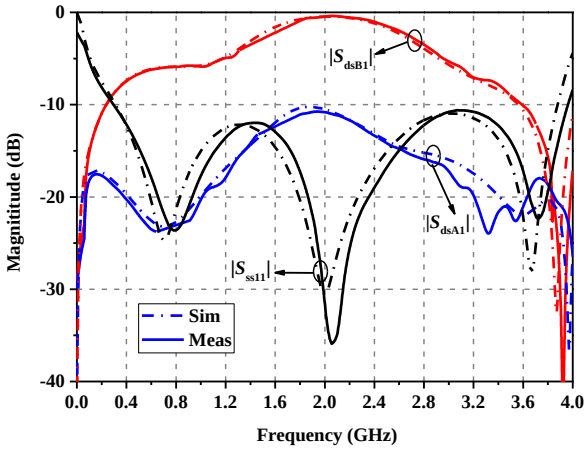

Fig. 10. Power transmission coefficients and the input port return loss.

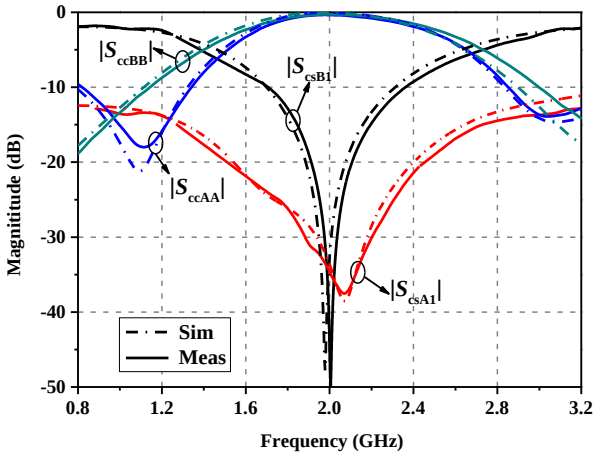

Fig. 11. Common-mode coefficient.

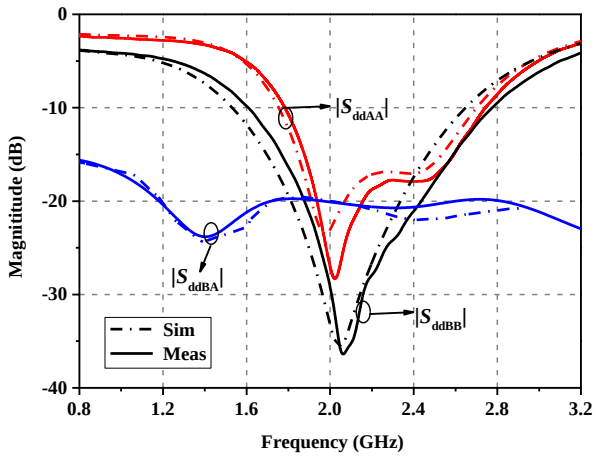

Fig. 12. Balanced ports return losses and the isolation.

The photograph of the power divider is as shown in Fig. 9 with the overall size of $0.28\,\lambda_g \times 0.95\,\lambda_g$. The simulation results are obtained using the HFSS software. The Agilent N5230A is used to measure this component with the frequency range of 0.0003–4 GHz with the OSLT calibration.

The curves of the power transmission coefficients and the input port return loss $|S_{ss11}|$ are given in Fig. 10. The measured impedance bandwidth is from 0.292 to 3.966 GHz with an FBW of 183.7%. The $|S_{ss11}|$ is measured as −31.53 dB at f_0. The $|S_{dsB1}|$ and $|S_{dsA1}|$ are measured as −10.81 and −0.45 dB at f_0, respectively, leading to a 10-dB PDR. Two transmission zeros at 0.8 and 3.72 GHz are generated.

As shown in Fig. 11, the measured CMSs at f_0 are 44 and 34 dB, respectively. The CMSs are better than 20 dB from 1.91 to 2.11 GHz, and 1.54 to 2.40 GHz, respectively.

Figure 12 gives the return losses of the two balanced ports and the isolation $|S_{ddBA}|$ between the two output ports. The $|S_{ddAA}|$ and $|S_{ddBB}|$ are measured as −27.04 and −29.18 dB, respectively. The bandwidth of the $|S_{ddAA}|$ below −10 dB is from 1.784 to 2.742 GHz (47.9%). The bandwidth of the $|S_{ddBB}|$ below −10 dB is from 1.608 to 2.776 GHz (58.4%). In the range of 0.8 to 3.2 GHz, the $|S_{ddBA}|$ is all below −15 dB, as shown in Fig. 12. At f_0 the isolation is measured as 20.06 dB. Figure 13 gives the simulation and measurement curves of the phase difference between S_{dsA1} and S_{dsB1}. It can be seen from Fig. 13, this SETB power divider has out-of-phase characteristics. The measured phase difference between the balanced ports is 180° ± 5° from 1.938 to 2.116 GHz.

The measurement PDR at the central frequency is 10.36 with a small shift from the target, which is due to the uncertainty of the microwave substrate parameters, the circuit size is $0.266\,\lambda_g^2$, meeting the target of $0.3\,\lambda_g^2$. The return losses at all ports are larger than 20 dB, meeting the design target. The input matching FBW is measured as 183.7% with a small shift from the target of 180%, which is due to the fabricate deviation.

The central frequency of the simulation $|S_{ddaa}|$ curve is located at 2.0 GHz. Referring to [26], for the ε_r uncertainty,

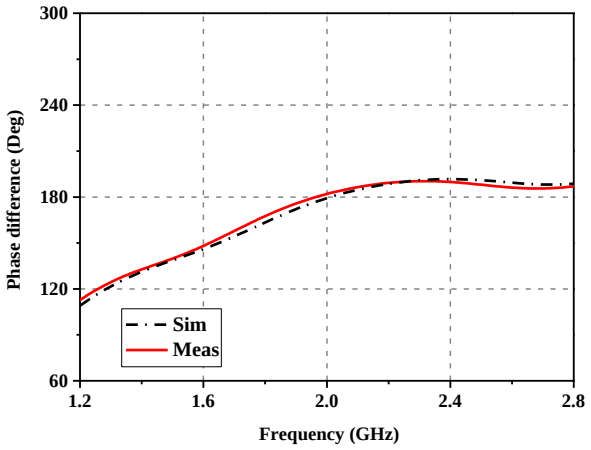

Fig. 13. Phase difference between S_{dsA1} and S_{dsB1}.

Refs.	f_0 (GHz)	PDR (dB)	RL (dB)	Impedance FBW (%)	CMS (dB)	Isolation (dB)	Fabrication	Circuit size ($\lambda_g \times \lambda_g$)
[9]	1.0	Equal	>25.68	~60	21.5	31.32	MS	0.09
[10]	1.53	Equal	15	~13	28	20	MS	0.19
[14]	2.0	3	>20	32	>30	>20	MS	0.317
[19]	5.9	Equal	>14	27	>30	>30	MS/SL	-
[20]	4.93	Equal	>13	79.6	27	>15	MS/SL	~1.26
[21]	4.0	Equal	>14	~137	>27	>15	MS/SL	0.723
[22]	3.26	Equal	>15.9	~22	28.5	>17.6	MS/SL	0.395
This work	**2.0**	**10**	**31.53**	**183.7**	**34**	**20.06**	**MS**	**0.266**

PDR: Power division ratio. RL: Return loss FBW: Fractional bandwidth. MS: Microstrip. SL: Slot

Tab. 3. Performance comparisons of the proposed circuit with previous works.

the parameters can be calculated as $2.205 \le \varepsilon_{eff} \le 2.285$, 99.161 mm $\le \lambda_g \le$ 100.944 mm, and the frequency shift range is 1.98 GHz $\le f \le$ 2.02 GHz. For the h uncertainty, the parameters can be calculated as $2.24 \le \varepsilon_{eff} \le 2.25$, 99.9 mm $\le \lambda_g \le$ 100.2 mm the frequency shift range is 1.998 GHz $\le f \le$ 2.002 GHz. The central frequency of the measurement curve is located at 2.02 GHz within the frequency shift range of the ε_r and h uncertainties, which is considered acceptable. Similarly, the frequency shift of $|S_{ddbb}|$ and $|S_{csB1}|$ is within the acceptable range, too. The central frequency of the simulation curve of $|S_{ss11}|$ is located at 2.0 GHz, however, the measured one is located at 2.038 GHz, except for the uncertainties of ε_r and h, the parasitic inductance generated by the hole could lead to the frequency shift of the $|S_{ss11}|$.

The comparisons among previous SETB power dividers are summarized in Tab. 3. Compared with the previous works in Tab. 3, the proposed SETB power divider has good matching characteristics at the central frequency. Besides, this work can provide a good CMS characteristic at the central frequency. Except for the power dividers in [9] and [10], the proposed power divider can provide a compact structure and the widest input matching bandwidth, which is due to the generation of two reflection zeros by the two λ/2 transmission lines and the coupled line with a short-circuited terminal, without other branches structures.

4. Conclusion

In this paper, a SETB power divider has been presented. Steps are given to guide the circuit design. By using the derived equations, the required power division ratio and the port matching can be realized. The proposed unequal power divider can provide a very wide impedance bandwidth to reduce the influence of undesired RF-signal-power reflections on the operation of the preceding active stage in the RF front end. For practical validation, a SETB power divider with 10-dB PDR has been fabricated and tested. All the ports can achieve good matching at the central frequency. For the input matching FBW, frequency shifts happened between the simulation and measurement curves, which are mainly caused by the uncertainty of the microwave substrate parameters. The differences are considered acceptable.

Acknowledgments

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