A Wide-band High-performance Voltage-controlled Oscillator for 5G IoT Wireless Communication

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Abstract. *A low phase noise and power-efficient class-B/C hybrid voltage-controlled oscillator (VCO) is presented for applying to 5G Internet of Things (IoT) wireless communication in this paper. The proposed three sets of switch capacitor array (SCA) are adopted first to widen the bandwidth by dividing the VCO output into eight overlapped frequency bands while maintaining the flexible frequency tuning. Then a multiple bias variable capacitor array (VCA) is designed to realize the fine-grain tuning of output frequency, which also improves the linearity within frequency-voltage tuning, the curvature variation in tunable gain, while minimizes the phase noise and stabilize tuning control on output frequency. After circuit implementation based on 180nm/1.2V CMOS standard process, the post-layout simulation results demonstrate that the proposed VCO achieves a wide frequency output from 4.63 GHz to 5.13 GHz, with consuming a total consumption of 0.19 mW at 1.2 V power supply voltage. The key phase noise is –115.1 dBc/Hz@1 MHz on the 4.82 GHz center frequency, and the figure of merit (FoM) value can reach up to –195.6 dBc/Hz, which can surpass the performance to comparable similar class VCO design cases.*

Keywords

LC voltage-controlled oscillator, Internet of Things communication, low phase noise, low power

1. Introduction

The rapid development of the Internet of Things (IoT) has brought about a pervasive presence of digital and intelligent technology in contemporary human society. IoT serves as the connective tissue linking an array of smart devices and sensors to the internet, facilitating the collection of diverse datasets for analysis and processing. This process enables the provision of a more intelligent and efficient lifestyle [1].

New protocols of higher transmission rates and capacity have been introduced to meet the requirements of IoT. However, this has led to new challenges concerning the performance requirements of RF analog circuits, specifically in terms of low voltage and low power consumption [2–4].Therefore, the design of a low-cost, low-power radio frequency transceiver hardware system is crucial due to the increasing demand for higher transmission rates and capacity in IoT technologies [5], [6]. In the operation of radio frequency transceivers, local oscillator (LO) signals, typically provided by phase locked loops (PLL), are indispensable components.

That is to say power consumption and noise performance of the PLL play an important role in the performance of IoT communication systems. The voltage-controlled oscillator (VCO) serves as the core circuit of the phase locked loop, consuming a considerable amount of energy [7], [8]. Thus, optimizing the performance of the phase locked loop is tantamount to improving the VCO performance [9].

Quite a few advanced technologies have been proposed to achieve low phase noise or power consumption. Literature [10] proposed a pulse tail feedback technique which can enhance both $1/f^2$ and $1/f^3$ noise simultaneously, leading to an overall reduction in phase noise. However, its frequency range is limited to a narrow range. Literature [11] adopting current reuse techniques contributed to a reduction in power consumption and phase noise levels. Literature [12] utilizes a constant and low tuning gain to achieve a lower phase noise. Literature [13] has designed an ultra-low-power width-band LC-VCO based on capacitor-inductor series shunting technology at the expense of increased power consumption. Existing VCOs primarily focus on addressing either power consumption or phase noise, with limited literature proposing a compromise that offers a VCO with superior overall performance.

The attainment of lower phase noise levels was facilitated by the utilization of constant and low tuning gain strategies. In order to enhance the transceiver performance by mitigating the impact of frequency pulling, VCO is required to cover the 4.8–5.0 GHz frequency band, which is twice the ISM frequency band. With the frequency range comprehensively scanned and captured the output signal is converted into quadrature signals via a frequency divider circuit for utilization in the transceiver.

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This work proposed a wide-band high-performance voltage-controlled oscillator for 5G IoT wireless communication, which achieves a static power consumption of 0.19 mW at a 1.2 V power supply voltage. At the central frequency of 4.82 GHz, the phase noise is measured to –115.1 dBc/Hz@1 MHz, resulting in an impressively significant FoM value of –195.6 dBc/Hz. The main contributions of this study are summarized as follows:

- A switchable capacitor array (SCA) and variable capacitor array (VCA) are introduced into LC resonant cavity to function the coarse and fine-grain frequency tuning.
- The VCA with eight optional sub-bands not only ensures more stable tuning voltage control by smaller tuning gain K_{vco}, but also expands the continuous tunable range with better output linearity in frequency switching.
- The smaller unit variable capacitance operated in each sub-band in SCA and VCA would greatly reduce phase noise induced by a large capacitor in traditional LC-VCO, while realizes power-efficiency due to sub-band-selective operating.
- A novel class B/C hybrid active circuit topology combining dynamic PMOS switch-pair and RC filter feedback is proposed to efficiently decrease phase noise and optimize power consumption.

The rests of this paper are organized as follows: Section 2 gives a general introduction of the traditional LC oscillator and circuit model. Section 3 presents the details of the proposed LC oscillator. Section 4 illustrates the layout design and its post-simulation results, power dissipation and FoM feature are performed between our proposed VCO and some other existed design cases. Some conclusions are drawn in Sec. 5.

2. Traditional LC Oscillator and Circuit Model

A traditional LC-type oscillator consists of a LC resonant cavity that generates constant amplitude oscillation outputs by consuming and converting energy, and an "active circuit" section powering the resonant cavity. The simplified circuit model is shown in Fig. 1.

Ideally, a resonant cavity would sustain undamped oscillations without energy loss during oscillation output. In actual circuits, inductors and capacitors are not ideal components due to process variation and nonideal effects such as material parasitic, leading to energy loss during circuit oscillation. Hence, for the convenience analysis, the LC tank is commonly regarded to be equivalent to a lumped parasitical load resistance R_P. As shown in Fig. 1, this resistance R_P, similar to a parasitic element, would result in heating and other energy losses, which causes continuous energy dissipation during oscillator operation.

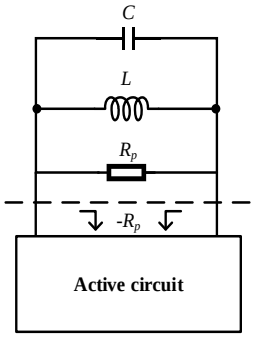


Fig. 1. A simplified negative resistance circuit model of LC oscillator.

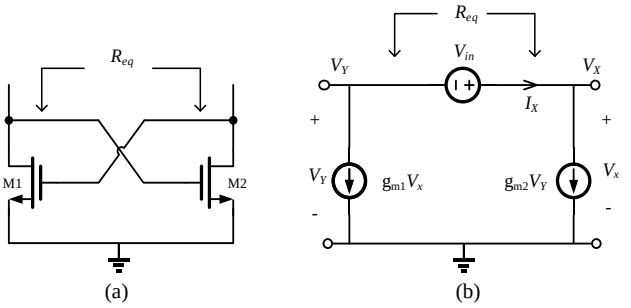


Fig. 2. A cross-coupled NMOS transistor pair as the equivalent negative resistance in a simple LC-oscillator (a) and its small-signal model (b).

Such dissipation leads to the eventual decay of potential energy and the cessation of oscillation. To counteract this effect, it is a standard manner to set with connecting a negative resistance of $-R_P$ (as illustrated in Fig. 1) across the resonant cavity to replenish the energy dissipated on R_P by the oscillation output.

Additionally, in order to simplify the analysis on principle of a conventional LC-VCO, as illustrated in Fig. 2(a), a cross-coupling transistor pair can be established to implement the "active circuit", while its small-signal equivalent circuit is presented in Fig. 2(b). Then, the following formulas can be easily obtained according to this equivalent circuit:

$$V_{in} = V_X - V_Y, \tag{1}$$

$$I_X = -g_{m1}V_X = g_{m2}V_Y. \tag{2}$$

By combining formulas (1) and (2), we can express V_{in} as

$$V_{in} = -I_X\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right). \tag{3}$$

Here, MOS transistor M1 and M2 in Fig. 2(a) have equal electrical parameters, so we can get that g_{m1} equals to g_{m2}. Finally, the equivalent input impedance R_{eq} (i.e., $-R_P$ in Fig. 1) for "active circuit" can be expressed as:

$$R_{eq} = \frac{V_X}{I_X} = -\frac{2}{g_m}, \quad (g_m = g_{m1} = g_{m2}). \tag{4}$$

Therefore, the continuous oscillating condition for this VCO circuit model can be inferred as below:

$$R_{\text{total}} = R_{\text{eq}} \parallel R_{\text{p}} = \frac{R_{\text{eq}} \times R_{\text{p}}}{R_{\text{eq}} + R_{\text{p}}} = \frac{R_{\text{p}} \times \left(-\frac{2}{g_{\text{m}}} \right)}{R_{\text{p}} - \frac{2}{g_{\text{m}}}}, \tag{5}$$

$$\begin{aligned} &\because R_{\text{p}} \times \left(-\frac{2}{g_{\text{m}}} \right) \le 0, \quad R_{\text{total}} \le 0, \\ &\therefore R_{\text{p}} - \frac{2}{g_{\text{m}}} \ge 0 \quad \Rightarrow \quad \frac{2}{g_{\text{m}}} \le R_{\text{p}}. \end{aligned} \tag{6}$$

3. The Proposed LC Voltage-controlled Oscillator

The proposed LC-VCO circuit, as depicted in Fig. 3, incorporates some key elements that are under meticulous design to optimize performance. Firstly, we innovated by implementing a hybrid Class B/C architecture to devise an active negative resistance network, where M1 and M2 constitute a Class-C structure, while M5 and M6 form a Class-B structure [14]. This topology enhances transconductance efficiency compared with the conventional single NMOS-coupled active circuit supply structures [15]. Additionally, the complementary topology facilitates the realization of symmetry tuning of the output oscillation waves, at the same time yielding a substantial power consumption reduction thanks to the Class-C operation. For the same current consumption, the theoretical phase noise improvement, compared to the standard differential-pair LC-tank oscillator, is 3.9 dB. Looked at in a different way, more than 50% current saving is achieved for the same phase noise level [26].

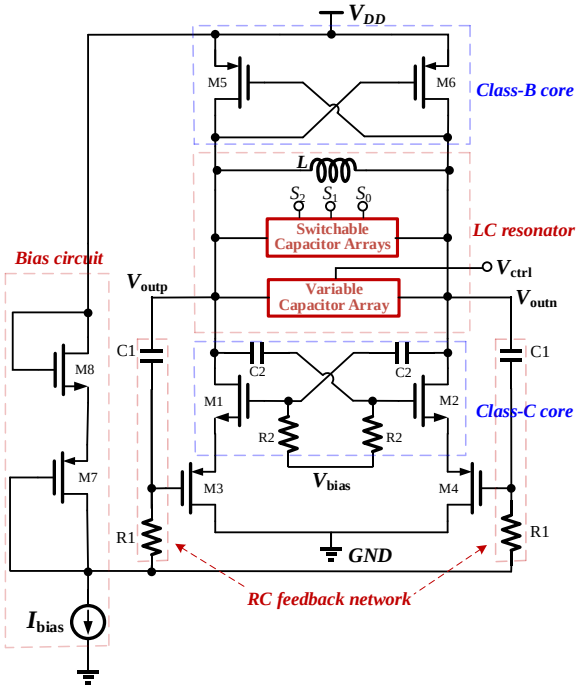


Fig. 3. Topology of our proposed LC-VCO circuit.

Device	Size (W/L)	Device	Size (W/L)/ Value
M1	60μm/180nm	M7	32μm/180nm
M2	60μm/180nm	M8	16μm/180nm
M3	40μm/180nm	R1	5.23 kΩ
M4	40μm/180nm	R2	1 kΩ
M5	120μm/180nm	C1	400 fF
M6	120μm/180nm	C2	50 fF

Tab. 1. All component parameters in the proposed LC-VCO circuit.

In bias sub-circuit, M7 and M8 are in conjunction with a current source to establish a reliable bias current I_{bias} that is provided for driving the core VCO. In addition, in core VCO topology, we add the PMOS pair of M3 and M4 to operate as a dynamic switch-pair. This topology constructs a low-impedance loop near the ground terminal, which effectively suppresses the tail noise injection into LC resonant tank and safeguards against phase noise degradation [16]. At same time, at the output port V_{outp} and V_{outn}, with incorporation of an RC filter feedback network, it would serve multiple purposes, of including high frequency noise filtering within output signal and selective frequency controlling. The specific configuration in resistance and capacitance value of this RC network can also determine the switching time of the PMOS transistors M3 and M4, thereby to enable precise adjustment of the output oscillation frequency. Table 1 presents the device sizes and parameter values for the LC-VCO circuit in this study.

The VCO's core resonant tank composes of an inductor L, a variable capacitor and a switchable capacitor array (SCA). In this case, the output frequency of the LC-VCO can be expressed as:

$$f = \frac{1}{2\pi\sqrt{L\left(C_{\text{VCA}} + C_{\text{SCA}}\right)}}. \tag{7}$$

The switchable capacitor array enables a fixable selection, i.e., grain-tuning on various frequency bands, ensuring compatibility with a wide range of applications within the 4.8 GHz ~ 5.0 GHz frequency coverage. Meanwhile, the variable capacitor facilitates fine-tuning in a certain frequency band on the output to meet specific requirements.

3.1 Switchable Capacitor Arrays (SCA) for Coarse Tuning

The proposed switchable capacitor array (SCA) is controlled by the external 3-bit digital signal (000~111) for coarse tuning, i.e., band selection within total eight sub frequency bands for the LC-VCO output. It is designed based on two primary design motivation and goals. First, it needs to guarantee that the VCO can operate with covering all the expected and necessary frequency tuning range under different process and temperature conditions. Second, it can realize the flexible and customization band division on the output frequency of VCO. As illustrated in Fig. 4, compared with a traditional VCO with a simple LC-tank topology carrying normally a larger variable capacitor,

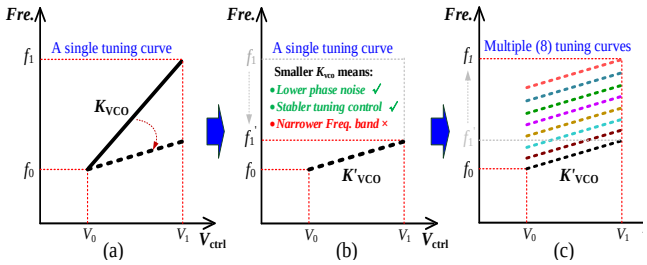


Fig. 4. Better frequency tuning feature based on dividing one single *f*-V curve into multiple curves: (a) Traditional single band in large K_{vco}; (b) Single band in small K'_{vco}; (c) Multiple sub-bands (8-band) in the same K'_{vco} in this paper.

by introducing a SCA module, which segments a single tuning curve (a) into eight sub-frequency bands (c), and then combining the relevant band control approach, the tuning gain of VCO, i.e., K_{VCO} can be decreased effectively. This topology contributes to ensure the stability of the tuning control while prevents excessive introduction of phase noise due to the smaller variable capacitors in SCA, ultimately leading to noise reduction [17–20].

As illustrated in Fig. 5, the proposed switchable capacitor array is composed of three frequency tuning units. Three core NMOS transistors M9, M10, M11 would operate as control switches within these tuning units during the band switching process. The resistors are employed for fine-grain tuning and configuring the output DC reference level for each frequency band. When the MOS switch is closed, the resistor is effectively connected in parallel with the MOS's on-resistance, thereby minimizing the influence of the on-resistance on the resonant cavity's *Q* value. Conversely, when the MOS switch is turned off, this resistor serves to stabilize the high voltage level at both ends of the switch, preventing leakage from the source and drain of the MOS switch and safeguarding the *Q* value from deterioration.

The capacitors maintain a fixed value to realize coarse tuning of the output frequency. In order to obtain 8 sub-bands, the capacitance values of different arrays were set in binary proportions ($C_3 = 2C_2 = 4C_1$). Three external logic control signals S_0, S_1 and S_2 drive the three switching transistors, which are switched on when *S* level is high. Simultaneously, the frequency-selecting capacitor is also introduced to engage and facilitate coarse tuning on the oscillating output. Furthermore, in order to maintain consistency on the output frequency across adjacent different frequency bands, proper and precise selection on these capacitance values is essential to ensure a 40% overlap between adjacent frequency bands.

For instance, considering an individual frequency tuning unit where the MOS transistor switch is conducting. In this case, the equivalent resistance and quality factor *Q* of the tuning unit can be expressed as:

$$Q = \frac{2}{\omega C R_{on}}, \tag{8}$$

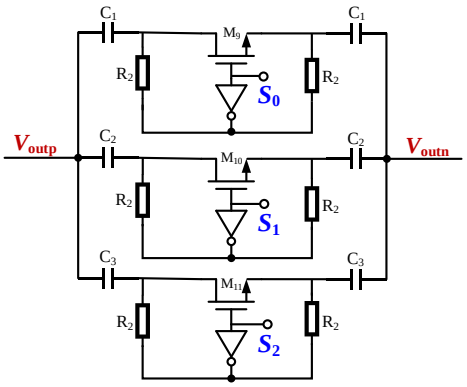


Fig. 5. The proposed switchable capacitor arrays (SCA).

$$R_{on} = \frac{1}{g_m} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})}. \tag{9}$$

To improve the quality factor *Q*, the on-resistance of the switch MOS transistor should be minimized as possible, according to (8) and (9), which necessitates an increase in the transistor channel size *W/L*. However, the expanding size of a transistor would result in heightened parasitic capacitance, which subsequently leads to a decrease in the output frequency of the VCO. Hence, the choice on appropriate size of the switch MOS transistor entails a trade-off that must be carefully weighed alongside the VCO performance considerations during the design.

3.2 Variable Capacitance Array (VCA) for Fine-grain Tuning

The variable capacitor array is controlled directly by the input control voltage V_{ctrl} and two bias voltages V_{bias1}, V_{bias2} for fine-grain tuning on the output frequency of the LC-VCO, of which the output oscillation frequency *f* and tuning gain K_{VCO} (denotes the variation value of output frequency caused by the unit control voltage change), can be denoted in the operating phase as:

$$f = \frac{1}{2\pi\sqrt{LC_{total}}}, \tag{10}$$

$$K_{VCO} = \frac{\partial f}{\partial V_{ctrl}} = \frac{\partial f}{\partial C_{total}} \times \frac{\partial C_{total}}{\partial V_{ctrl}} = \frac{-1}{4\pi C_{total}\sqrt{LC_{total}}} \times \frac{\partial C_{var}}{\partial V_{ctrl}} \tag{11}$$

where C_{total} is the equivalent total capacitance of the LC resonant cavity; C_{var} is the variable capacitance value in traditional VCO; V_{ctrl} is the input control voltage, which is also control voltage of the VCA module for fine-grain frequency tuning. We can see that K_{VCO} is proportional to the value variation of C_{var} from (11).

As the practical operating behavior of a VCO, the large variable capacitance shows nonlinear feature along with the input control voltage while introduces more phase noise. Therefore, stabilizing and improving the linear proportional relationship between the capacitance and control

voltage for the variable capacitance [21], [22] is very essential for minimizing the significant variation on *f*-*V* tuning curve. Based on this consideration, as shown in Fig. 6, a variable capacitor array (VCA) with smaller unit capacitors and symmetry topology on the *Y*-axis is proposed. In the VCA module, it consists of two selfsame capacitor sets, Cap. set #1 and Cap. set #2. Then, V_{bias1} and V_{bias2} serve as the input bias control voltages via resistor pair R_1, variable capacitor pair C_{var} and capacitor pair C_1, to control the shift and superposition of *C*-*V* tuning ranges of two capacitor sets in VCA in order to realize finally the extension of the tunable capacitance. In actual operating, we set V_{bias1} and V_{bias2} as to 0 V and 0.6 V as fixed values, while C_1 = 2.4 pF and the layout dimension W/L of unit variable capacitance C_{var} is valued 10 µm/1 µm.

As illustrated at left in Fig. 7, by applying two bias voltages 0 V and 0.6 V first for V_{bias1} and V_{bias2}, respectively in VCA, two *C*-*V* curves achieve "equivalent right shift" of the middle “linear region”, i.e., effective tunable range of *C*-*V* curve, which broadens the voltage tuning range of the variable capacitance and facilitates a more precise (namely fine-grain) adjustment of the output frequency of the proposed VCO. Moreover, based on this superposition effects of two capacitor sets, the final equivalent *C*-*V* curve of the “integrated” capacitance of VCA also becomes more linear, as right curve sketch of Fig. 7, that means that a full-scale control of input voltage V_{ctrl} of 0 V~1.2 V can be realized effectively, thereby the frequency tunable range (FTR) is expanded accordingly.

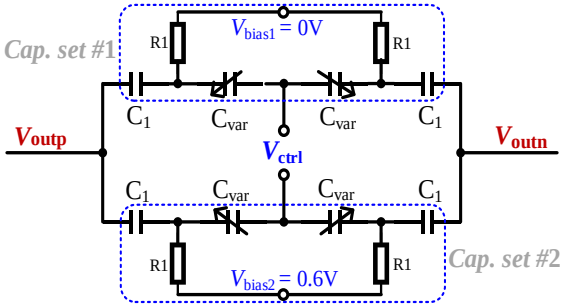


Fig. 6. The proposed variable capacitor array (VCA) consisted of two variable capacitor sets.

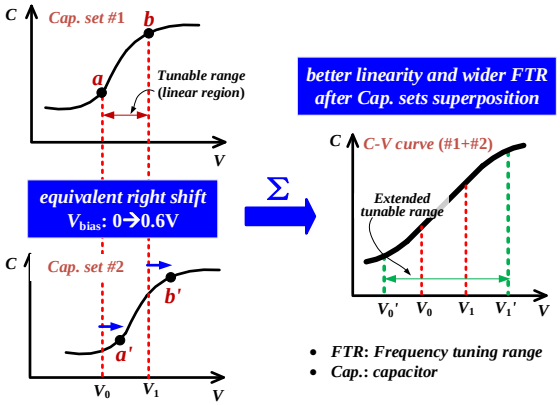


Fig. 7. *C*-*V* curve of VCA on a more linear scale based on superposition effects of two capacitor sets by different external biasing control.

Additionally, this topology leads to a reduction on slope variation of K_{VCO} [23–25], ultimately resulting in a more stable and easily tuning control on the output frequency.

4. Physical Design and Performance Verification

The back-end design of the proposed overall LC-VCO is implemented by 180 nm/1.2 V CMOS standard process. The final layout view of the VCO core, with excluding the bias circuit, is illustrated in Fig. 8. A symmetrical placement and routing are performed to realize approximately equal parasitic effects for improving the performance. The layout dimension is 0.47 mm × 0.28 mm. Afterward, the parasitic parameters are extracted and then the post-layout simulation is performed to evaluate the performance of the nearly-final circuit product after tape-out.

Based on the post-layout simulation results, with an operating supply voltage of 1.2 V and a full-scale input control voltage V_{ctrl} of 0 V–1.2 V, first, as shown in Fig. 9, we can observe a normal oscillating sine waveform as VCO output in time-domain transient simulation. And then, via the flexible manipulation of the on/off states of three logic switches (S_0, S_1, S_2) in SCA (Fig. 5), as drawn in Fig. 10, it can achieve the 8 sub-frequency band outputs as our design expectation. Also, a monotone increasing trend for each sub-band frequency tuning curve can be observed along with a uniform changing of input V_{ctrl}. The most important information from Fig. 10 is that, to all of the

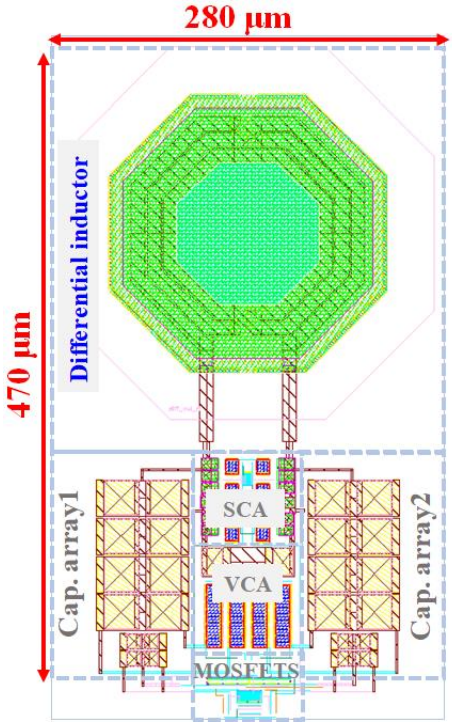


Fig. 8. The layout view of overall LC-VCO circuit.

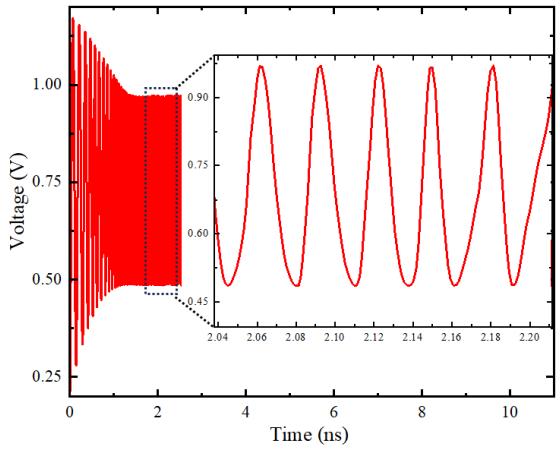


Fig. 9. The transient sim. based output waveform at oscillation frequency of 5 GHz of the proposed VCO.

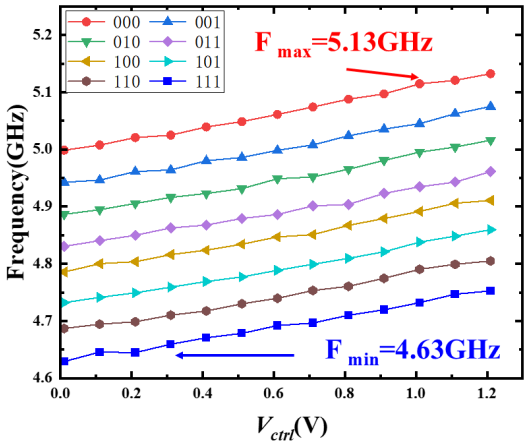


Fig. 10. Final 8-sub frequency band outputs of the proposed LC-VCO controlled by 3-bit logic code of SCA (coarse tuning for sub-band selection first) and input control voltage of VCA (fine-grain tuning for precise frequency regulation).

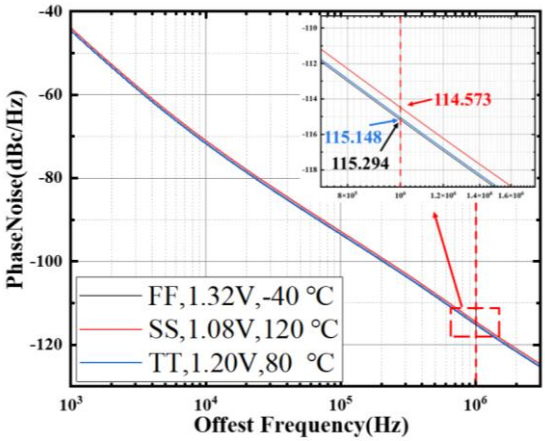


Fig. 11. PVT variation feature of phase noise.

eight sub-band curves, it is exhibited a frequency overlapping of up to 50% between adjacent sub-bands, i.e., the maximum frequency value of the lower curve line can reach or beyond the middle value of the adjacent upper line. This observable overlapping ensures high-precision wide-band continuous frequency output within the oscillating range of 4.63 GHz–5.13 GHz according to the simulation analysis.

Additionally, the PVT corners are run out and the result is shown in Fig. 11. It indicates a phase noise of –115.1 dBc/Hz at the 1 MHz frequency offset point, which represents a good anti-noise performance of the proposed LC-VCO. Moreover, a common statistical variation analysis regarding to output central frequency and phase noise is performed for verifying robustness of the proposed VCO. As shown in Fig. 12, we run 200 times standard Monte-Carlo simulations, and then according to the simulated values of Std Dev. and Mean in figure, we can further calculate 3σ error by standard formula "3(Std Dev./Mean)×100%". The final 3σ values are 0.19% and 0.58% for f_c and phase noise, respectively. It is also confirmed the proposed VCO circuit is significantly robust by showing superior feature in anti-variability and anti-noise.

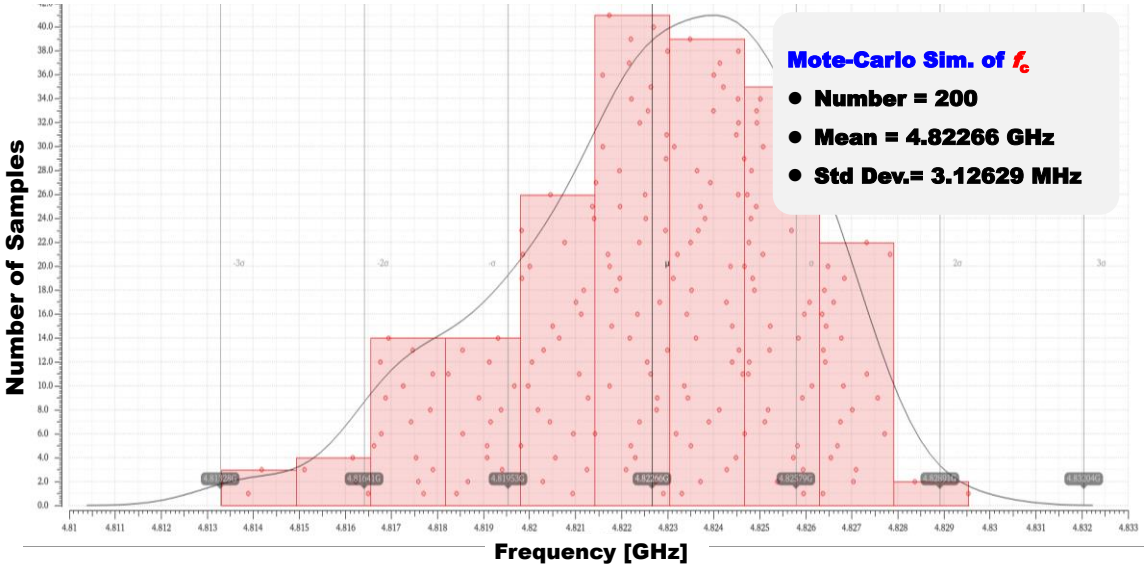
To conduct a thorough and comprehensive performance comparison for the proposed LC-VCO, we employ the figure of merit (FoM) factor, which considers all of the basic traditional performance evaluation parameters such as center frequency, tuning range, phase noise, and power consumption. The computation formula of FoM is as follows

$$\mathrm{FoM} = L(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left(\frac{P}{1\mathrm{mW}}\right). \quad (12)$$

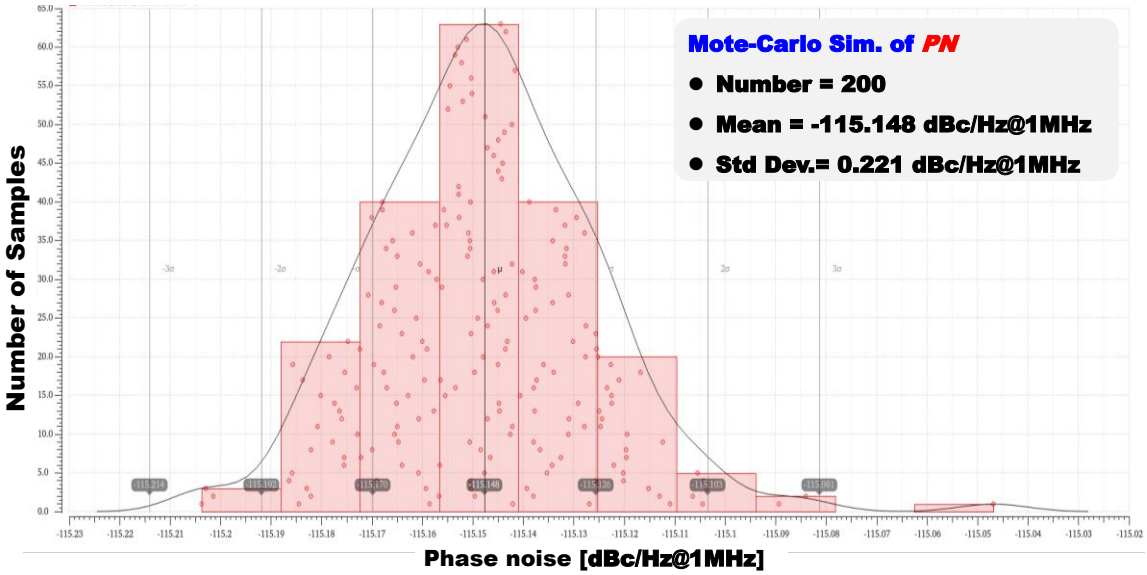
Furthermore, Table 2 compares the performance metrics of the proposed LC-VCO with other existing VCO design cases. With the moderate acceptable frequency range and phase noise under 1.2 V power supply voltage within the comparable six VCO design cases, the best FoM value –195.6 dBc/Hz due to the significantly remarkable power-efficient feature consuming only 0.19 mW demonstrates that LC-VCO our proposed obviously offers a superiority in circuit feature with significant comprehensive performance.

5. Conclusion

This paper presents a high-performance LC-VCO circuit using 180nm/1.2V standard CMOS technology. The post-layout simulation results show a static power consumption of 0.19 mW at a 1.2 V power supply voltage. At the central frequency of 4.82 GHz, the phase noise is measured to –115.1 dBc/Hz@1 MHz, resulting in an impressively significant FoM value of –195.6 dBc/Hz. The dimension of the overall LC-VCO circuit is 0.47 mm × 0.28 mm. With its excellent characteristics of relatively low power consumption, wide tuning range, and low phase noise, the proposed LC-VCO meets the requirements such as 5G and Wi-Fi IoT communication applications as clock generator and frequency synthesizer in high-performance RF wireless transceiver systems.



(a)



(b)

Fig. 12. 200 times Monte-Carlo simulation of output central frequency f_c and phase noise feature based on pre-simulation: (a) f_c; (b) Phase noise.

Item References	Technology [nm]	Power Supply [V]	Freq. Range [GHz]	Power Dissipation [mW]	Phase noise [dBc/Hz@1 MHz]	FoM [dBc/Hz]
[1]	130	0.8	2.18~2.41	0.26	–114.7	–188.2
[3]	65	0.8	2.43~2.53	0.31	–117.5	–189.6
[7]	130	1.2	2.16~5.13	5.14	–116.8	–183.9
[8]	180	1.5	2.60~4.40	5.48	–125.0	–184.5
[13]	90	1.2	1.13~1.90	1.06	–118.4	–181.9
[15]	180	1.2	4.76~5.33	1.85	–115.1	–186.4
This work	**180**	**1.2**	**4.63~5.13**	**0.19**	**–115.1**	**–195.6**

Tab. 2. Comparisons of performance metrics of the proposed LC-VCO with other design cases in modern literature.

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Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

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